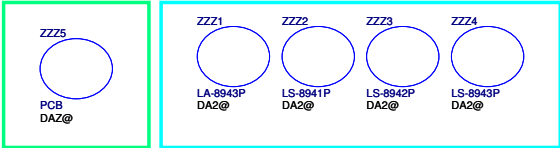


Compal Confidential

Model Name : Q1VZC
File Name :LA-8943P
BOM P/N:43



Compal Confidential

CHROME M/B Schematics Document

Intel Sandy Bridge ULV Processor + Panther Point PCH

2012-08-10

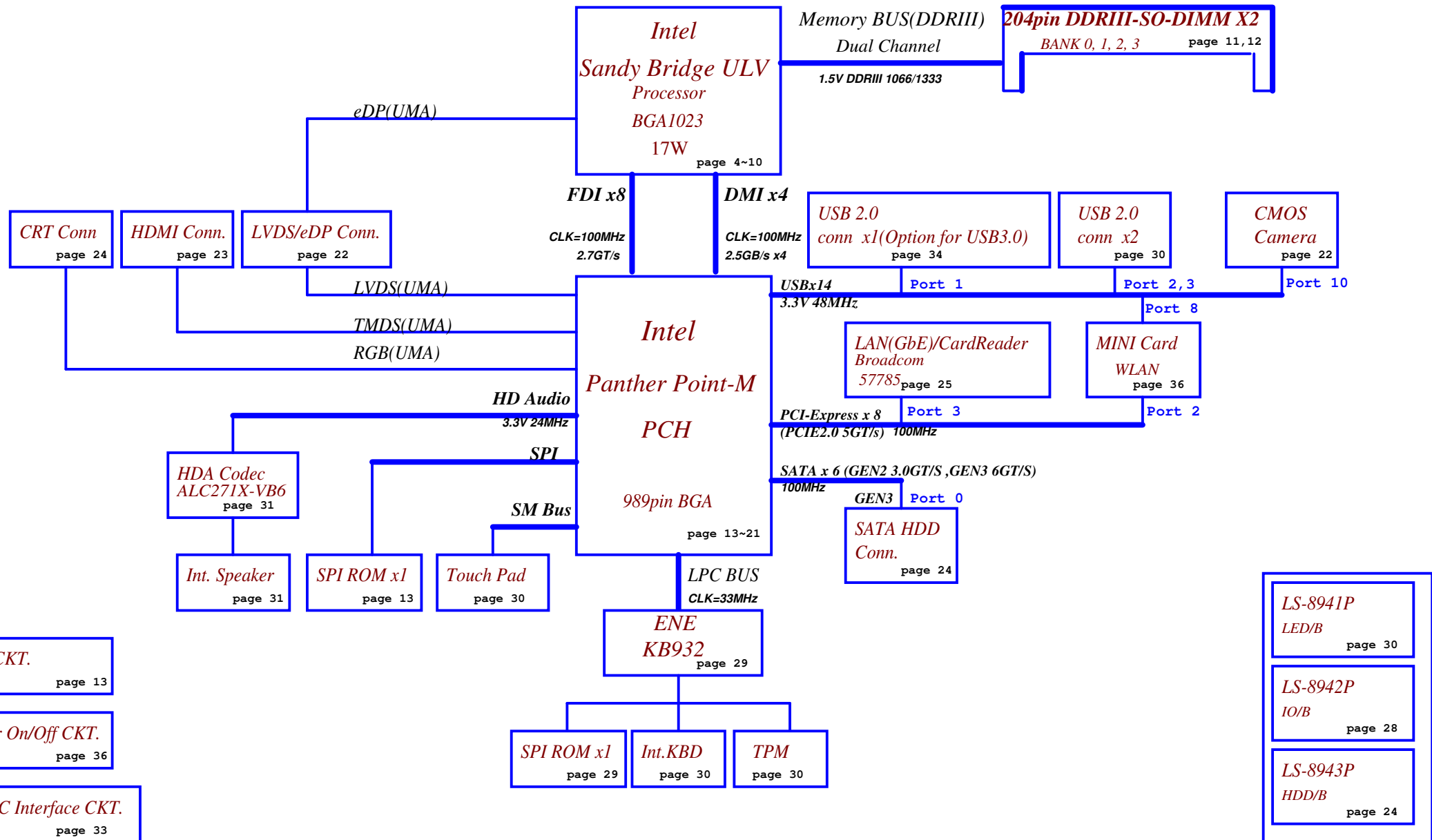
REV : 1 . 0

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				CHROME M/B LA-8943P Schematic	0.1
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Model Name : Q1VZC

File Name :LA-8943P



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				CHROME M/B LA-8943P Schematic	
				Date: Friday, August 10, 2012	Sheet 2 of 45
				Rev	0.1

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for CPU	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON
+VCCSUS3_3	+3VALW to +VCCSUS3_3 power rail for PCH (Short Jump)	ON	ON	OFF
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON
+5VREF_SUS	+5VALW to +5VREF_SUS power rail for PCH (Short resister)	ON	ON	OFF
+5VS	+5VALW to +5VS switched power rail	ON	ON	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

PCH SM Bus address

Device	Address
ChannelA	DIMM0 A0 1010 000X JDIMM1(STD)
ChannelB	DIMM0 B0 1010 010X JDIMM2(REV)

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
	Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

BTO Option Table	
BTO Item	BOM Structure
Celeron 867	C867@
Celeron 877	C877@
Unpop	@
eDP Panel	EDP@
LVDS Panel	LVDS@
Connector	CONN@
USB3 Only	USB3@
Deep S3	DS3@
Normal S3	S3@
Intel i5/i7 CPU only	I57@
Celeron/Pentium/i3 CPU only	CP3@

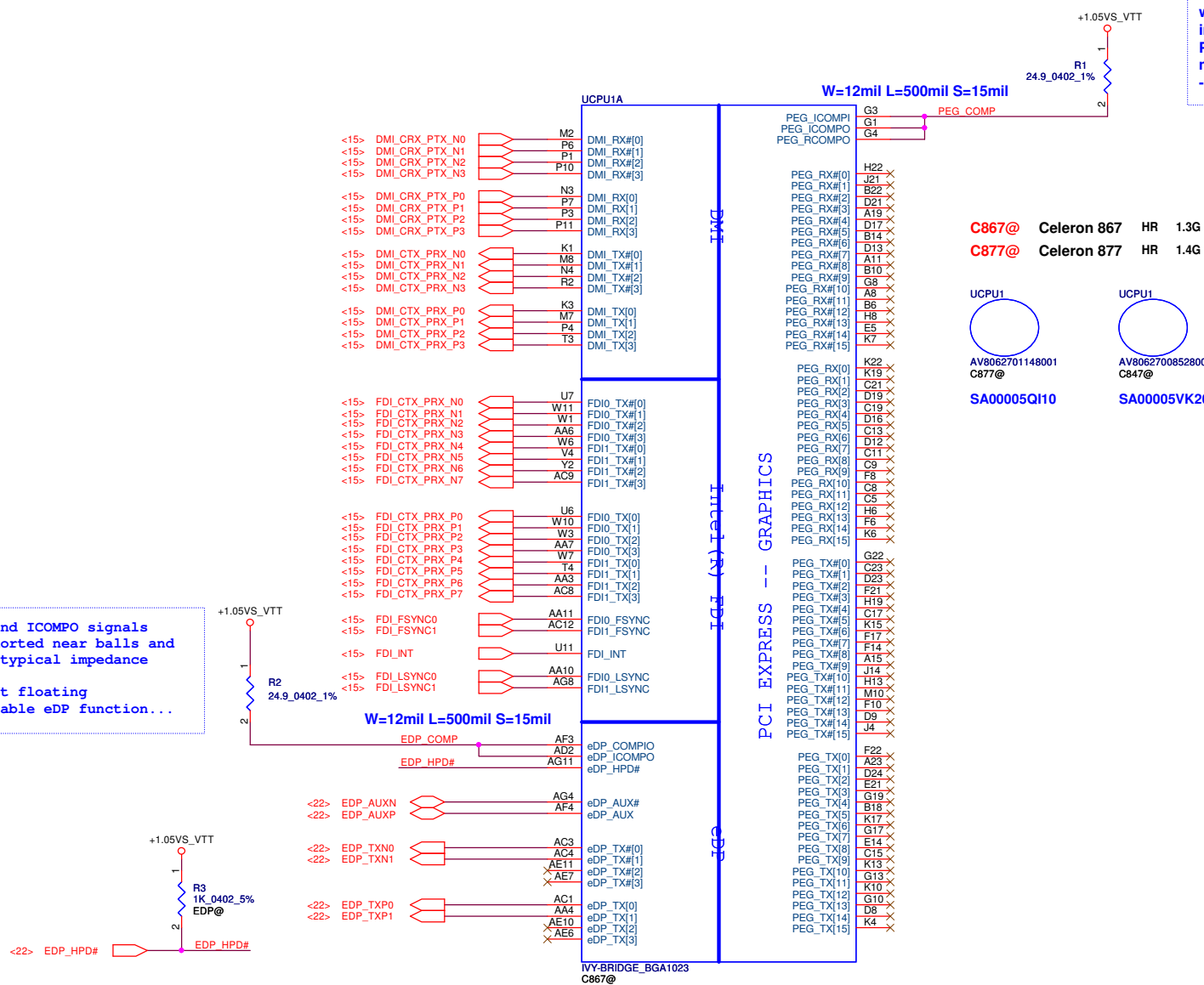
USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	
		1	USB 2.0(Options for USB3.0)
		2	USB port(Left 2.0)
	UHCI1	3	USB Port(Left 2.0)
		4	
	UHCI2	5	
		6	
EHCI2	UHCI3	7	
		8	Mini Card(WLAN)
		9	
	UHCI4	10	Camera
		11	
	UHCI5	12	
		13	

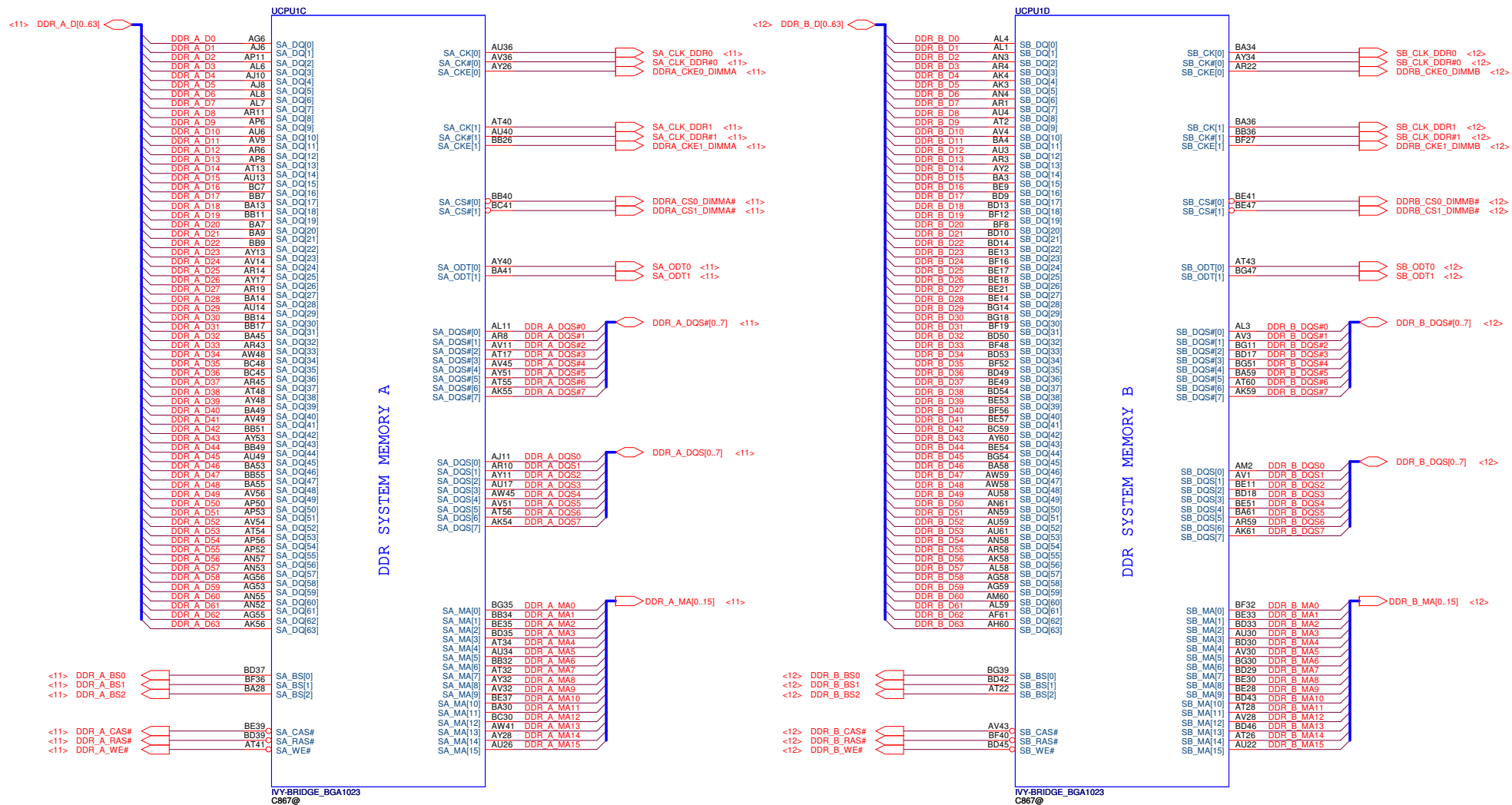
USB 3.0	Port	
XHCI	1	
	2	USB Port(Right 3.0)
	3	
	4	

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms can't be left floating ,even if disable eDP function...

PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



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Size	Custom	Document Number	CHROME M/B LA-8943P Schematic	Rev	0.1
Date:	Friday, August 10, 2012	Sheet	4	of	45

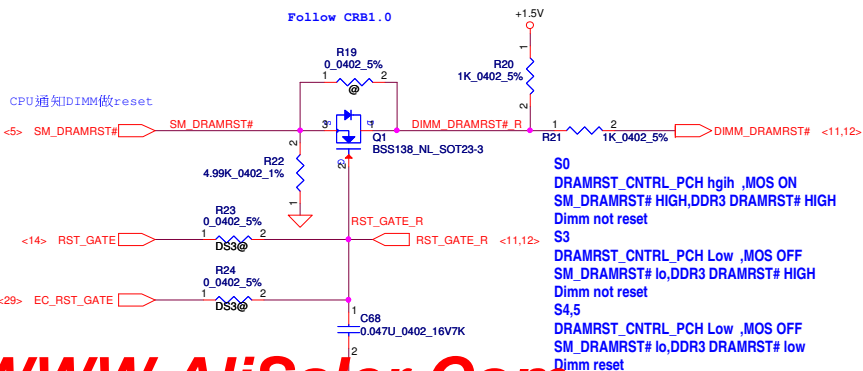


DDR SYSTEM MEMORY A

DDR SYSTEM MEMORY B

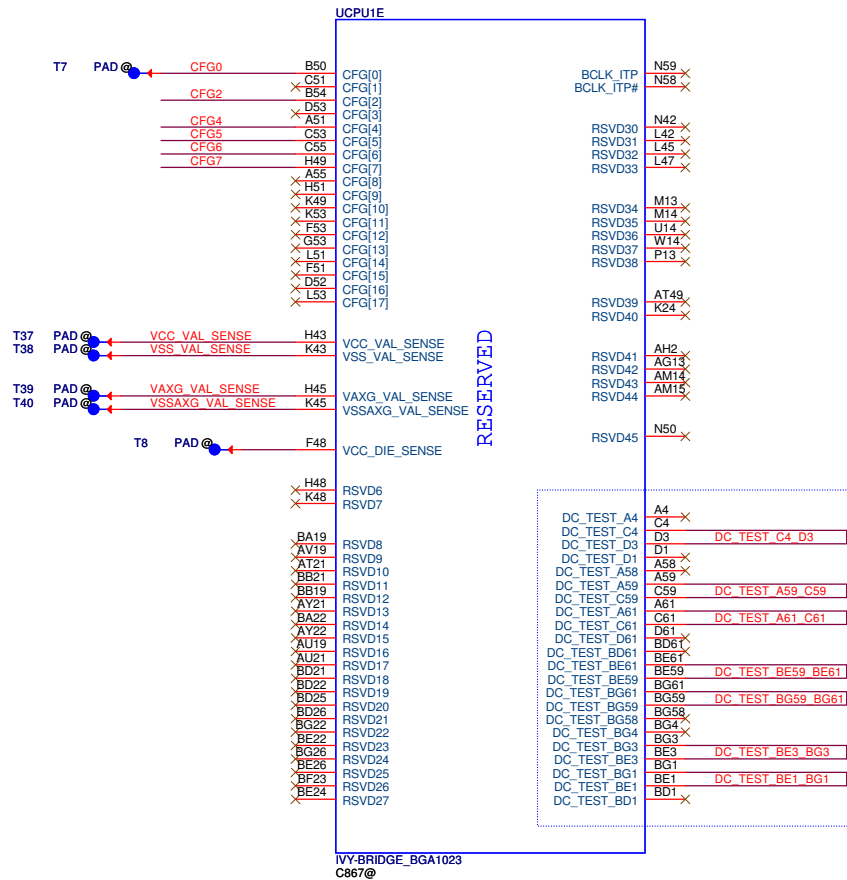
IVY-BRIDGE_BGA1023
C867@

IVY-BRIDGE_BGA1023
C867@



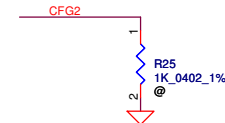
S0
DRAMRST_CNTRL_PCH hgh, MOS ON
SM_DRAMRST# HIGH,DDR3 DRAMRST# HIGH
Dimm not reset
S3
DRAMRST_CNTRL_PCH Low ,MOS OFF
SM_DRAMRST# lo,DDR3 DRAMRST# HIGH
Dimm not reset
S4,5
DRAMRST_CNTRL_PCH Low ,MOS OFF
SM_DRAMRST# lo,DDR3 DRAMRST# low
Dimm reset

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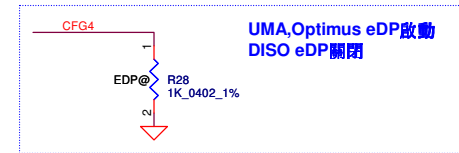


These pins are for solder joint reliability and non-critical to function. For BGA only.

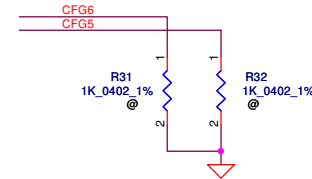
CFG Straps for Processor



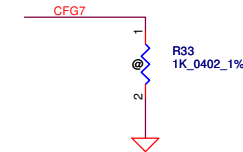
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition ★ 0: Lane Reversed



eDP enable	
CFG4	★ 1: Disable 0: Enable



PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) 1x16 PCI Express ★ 10: 2x8 PCI Express 01: Reserved 00: 1x8,2x4 PCI Express



PEG DEFER TRAINING	
Tacoma_Fall2 1.0 P.12	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

INTEL Recommend VCC
4*470uF,12*22uF(0805) and 35*2.2uF(0402)
PD0.8
CAP at P.51

ULV type
DC 33A

UCPU1F

POWER

8.5A

+1.05VS_VTT

For DDR

INTEL Recommend VCCIO
2*330uF,10*10uF(0603) and 26*1uF(0402)
PD0.8
CAP at P.51

For PEG

VCCIO_SEL after Ivy bridge ES2 Voltage support

BC22	*	1/NC : (Default) +1.05VS_VTT
		0: +1.0VS_VTT

Place the PU
resistors close to CPU

Place the PU
resistors close to VR

Should change to connect form
power circuit & layout differential
with VCCIO_SENSE.

Check list 1.5

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Issued Date		Deciphered Date		PROCESSOR(5/7) PWR,BYPASS	
2012/03/21		2013/03/21		Size	Rev
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				Date:	Friday, August 10, 2012
				Sheet	8 of 45

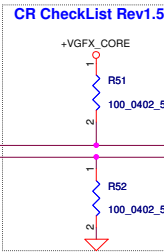
INTEL Recommend VAXG
2*470uF,6*22uF(0805) and 6*10uF(0603)
11*1U(0402)
PD0.8

INTEL Recommend VCCPLL
1*330uF,2*1uF(0402)
PD0.8

SGA00001700 S POLY C 220U
220U 2.5V M B2 ESR35 TPE H1.9

SGA20331E10 S POLY C 330U
2V Y D2 LESR9M EEFSX H1.9

INTEL Recommend VCCSA
1*330uF,5*10uF(0603) ,5*1uF(0402)
PD0.8



Place BOT OUT Conn

Place TOP IN BGA

Place BOT OUT BGA

POWER

UCPU1G

DC 16A

AA46 VAXG[1]
 AB47 VAXG[2]
 AB50 VAXG[3]
 AB51 VAXG[4]
 AB52 VAXG[5]
 AB53 VAXG[6]
 AB55 VAXG[7]
 AB56 VAXG[8]
 AB58 VAXG[9]
 AC61 VAXG[10]
 AD47 VAXG[11]
 AD48 VAXG[12]
 AD50 VAXG[13]
 AD52 VAXG[14]
 AD53 VAXG[15]
 AD55 VAXG[16]
 AD56 VAXG[17]
 AD58 VAXG[18]
 AD59 VAXG[19]
 AD59 VAXG[20]
 AE46 VAXG[21]
 F47 VAXG[22]
 F47 VAXG[23]
 P48 VAXG[24]
 P50 VAXG[25]
 P51 VAXG[26]
 P52 VAXG[27]
 P53 VAXG[28]
 P55 VAXG[29]
 P56 VAXG[30]
 P61 VAXG[31]
 T48 VAXG[32]
 T58 VAXG[33]
 T59 VAXG[34]
 T61 VAXG[35]
 U46 VAXG[36]
 V47 VAXG[37]
 V48 VAXG[38]
 V50 VAXG[39]
 V51 VAXG[40]
 V52 VAXG[41]
 V53 VAXG[42]
 V55 VAXG[43]
 V56 VAXG[44]
 V58 VAXG[45]
 V59 VAXG[46]
 W50 VAXG[47]
 W51 VAXG[48]
 W52 VAXG[49]
 W53 VAXG[50]
 W55 VAXG[51]
 W56 VAXG[52]
 W61 VAXG[53]
 Y48 VAXG[54]
 Y61 VAXG[55]
 Y61 VAXG[56]

GRAPHICS

DDR3 - 1.5V RAILS

SENSE LINES

1.8V RAIL

SA RAIL

SENSE LINES

VCCSA VID Lines

VREF
 SM_VREF
 SA_DIMM_VREFDQ
 SB_DIMM_VREFDQ

5A

VDDQ[1] AJ28
 VDDQ[2] AJ33
 VDDQ[3] AJ36
 VDDQ[4] AL30
 VDDQ[5] AL34
 VDDQ[6] AL38
 VDDQ[7] AL42
 VDDQ[8] AM33
 VDDQ[9] AM36
 VDDQ[10] AM40
 VDDQ[11] AN30
 VDDQ[12] AN34
 VDDQ[13] AN38
 VDDQ[14] AR26
 VDDQ[15] AR28
 VDDQ[16] AR30
 VDDQ[17] AR32
 VDDQ[18] AR34
 VDDQ[19] AR36
 VDDQ[20] AR40
 VDDQ[21] AV41
 VDDQ[22] AW26
 VDDQ[23] BA40
 VDDQ[24] BB28
 VDDQ[25] BC33
 VDDQ[26]

QUIET RAILS

SENSE LINES

VCCSA VID Lines

VCCDQ[1] AM28
 VCCDQ[2] AN26

VDDQ_SENSE BC43
 VSS_SENSE BA43

VCCSA_SENSE U10

VCCSA_VID[0] D48
 VCCSA_VID[1] D49

IVYBRIDGE_BGA1023 C867@

+V_SM_VREF should have 20 mil trace width

INTEL Recommend VDDQ
1*330uF,8*10uF(0603) ,10*1uF(0402)
PD0.8

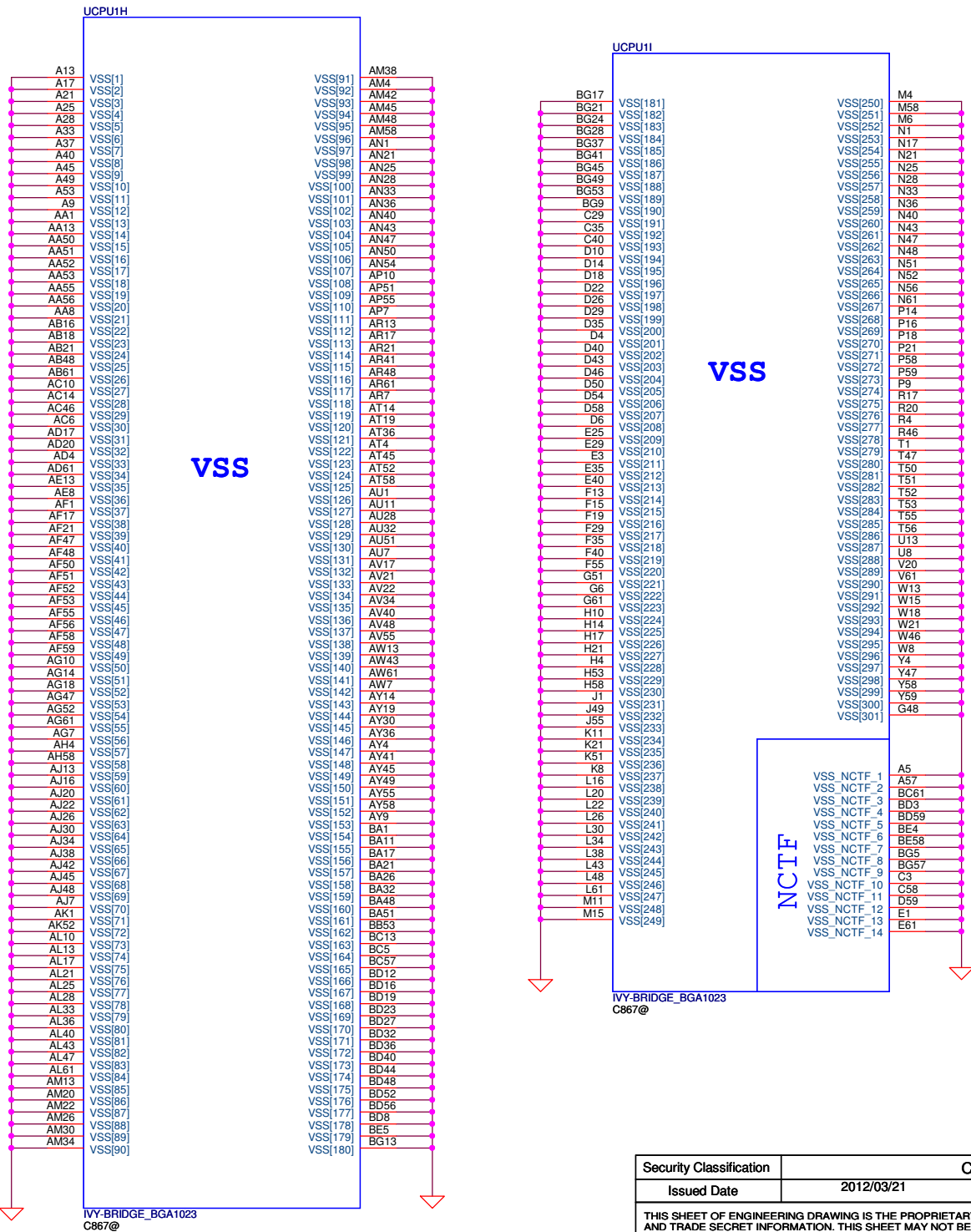
Place TOP IN BGA

Place BOT OUT BGA

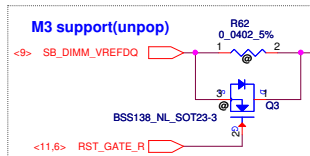
SGA20331E10 S POLY C 330U
2V Y D2 LESR9M EEFSX H1.9

CPU EDS1.3 P.93
VCCSA_VID0 Must PD

VCCSA				
VID0	VID1	Vout	HR	CR
0	0	0.9V	V	V
0	1	0.85V	V	V
1	0	0.775V	X	V
1	1	0.75V	X	V



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								PROCESSOR(7/7) VSS	
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Customer						Document Number		Rev	
						CHROME M/B LA-8943P Schematic		0.1	
Date:						Friday, August 10, 2012		Sheet 10 of 45	



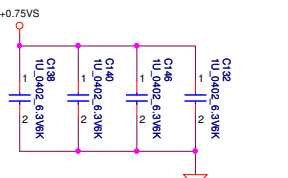
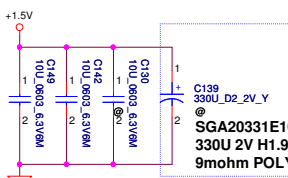
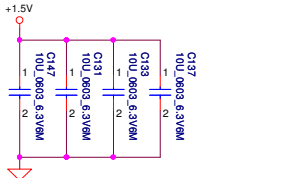
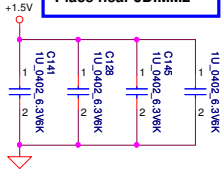
DDR_B_DQS#[0..7] <6>

DDR_B_DQS[0..7] <6>

DDR_B_D[0..63] <6>

DDR_B_MA[0..15] <6>

Layout Note:
Place near JDIMM2



Layout Note:
Place near JDIMM2.203,204

All VREF traces should
have 10 mil trace width

<6> DDRB_CKE0_DIMMB

<6> DDR_B_BS2

<6> SB_CLK_DDR0

<6> SB_CLK_DDR#0

<6> DDR_B_BS0

<6> DDR_B_WE#

<6> DDR_B_CAS#

<6> DDRB_CS1_DIMMB#

<6> DDRB_CKE1_DIMMB

<6> DDR_B_BS1

<6> DDR_B_RAS#

<6> DDRB_CS0_DIMMB#

<6> SB_ODT0

<6> SB_ODT1

<6> DDR_B_D32

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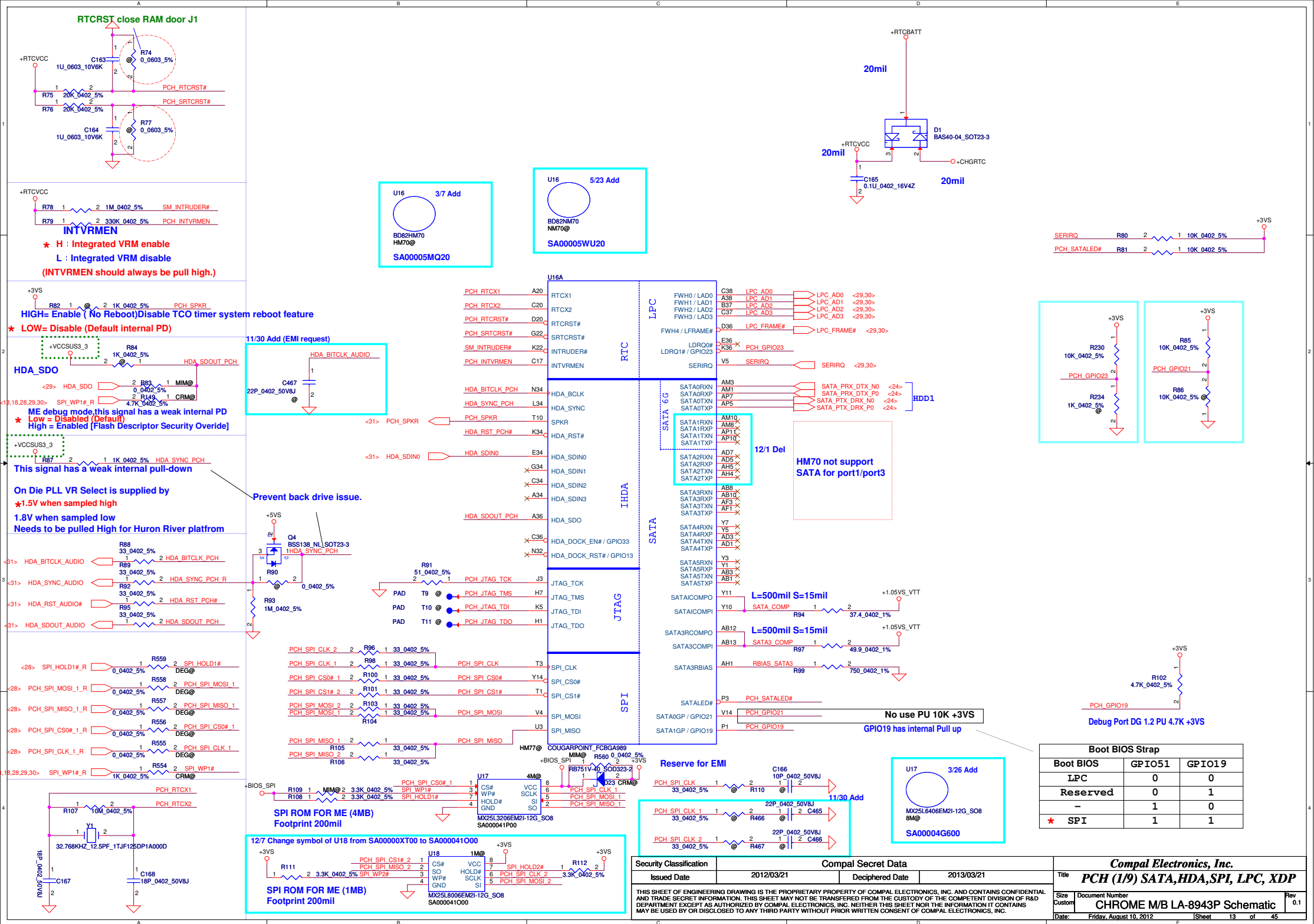
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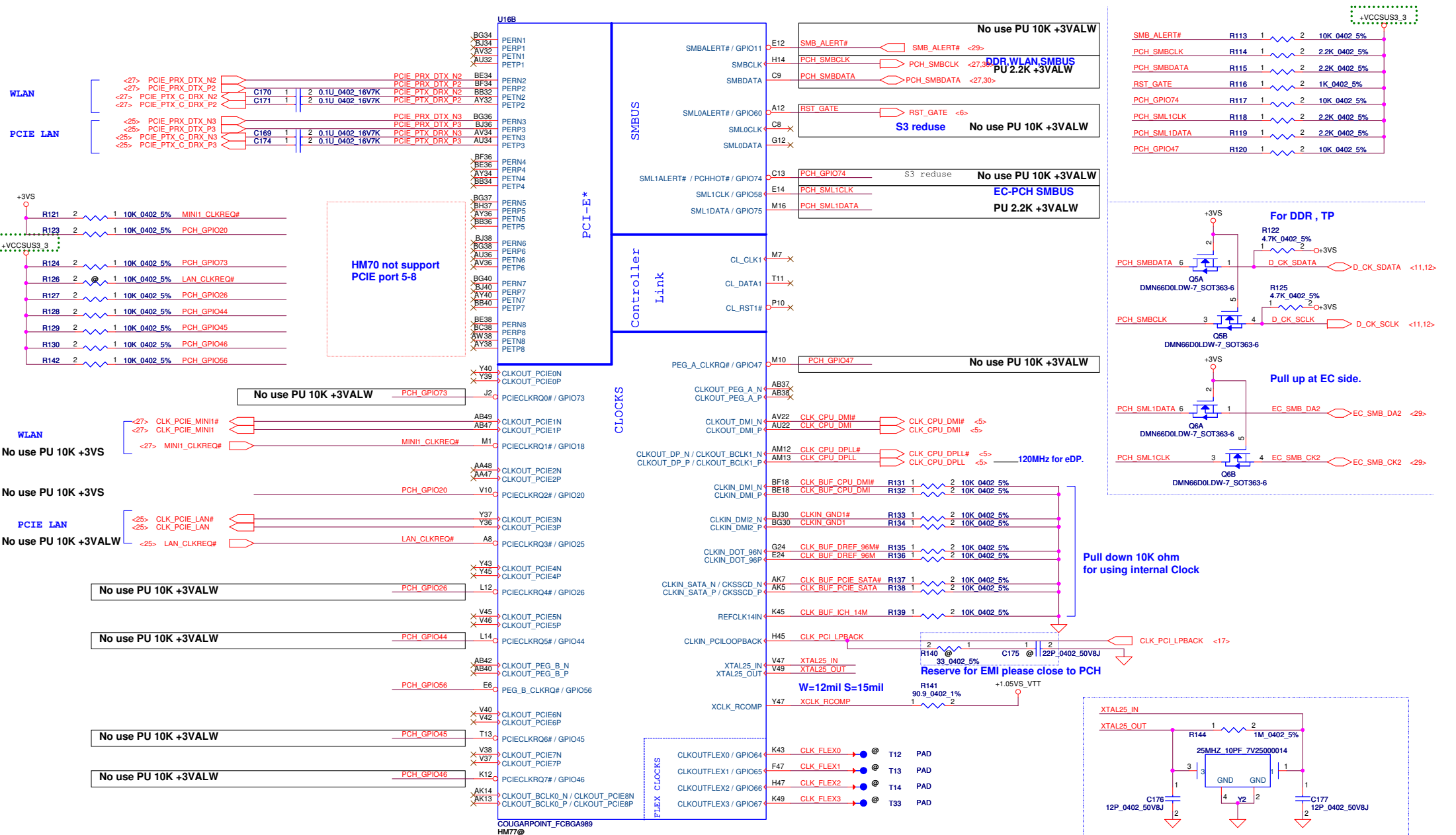
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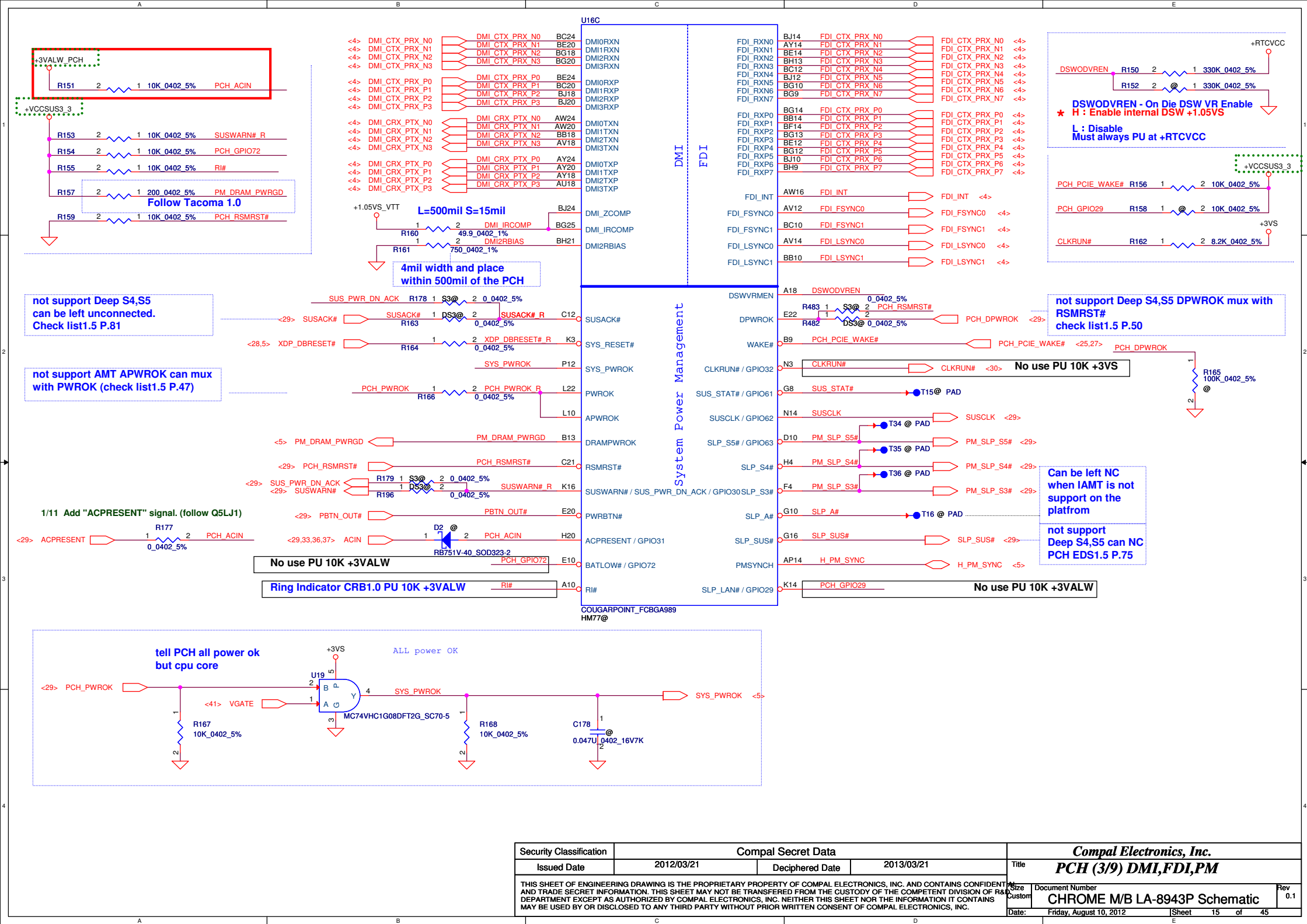
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<6> DDR_B_D260

<6>







<29> ENBKL < ENBKL R169 2 1 0 0402 5% IGPU BKLT EN

Change to eDP only

3VS

R170 1 LVDS @ 2 2.2K 0402 5% CTRL CLK

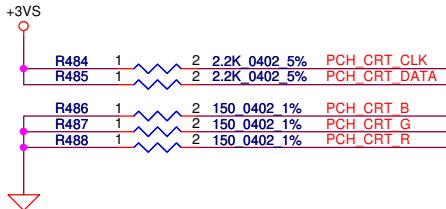
R172 1 LVDS @ 2 2.2K 0402 5% CTRL DATA

UMA LVDS DDC

R174 1 LVDS @ 2 2.2K 0402 5% PCH LCD CLK

R175 1 LVDS @ 2 2.2K 0402 5% PCH LCD DATA

LVDS disable:
DATA/Clock/Control an NC
VCC_TX_LVDS,VCCA_LVDS PD to GND



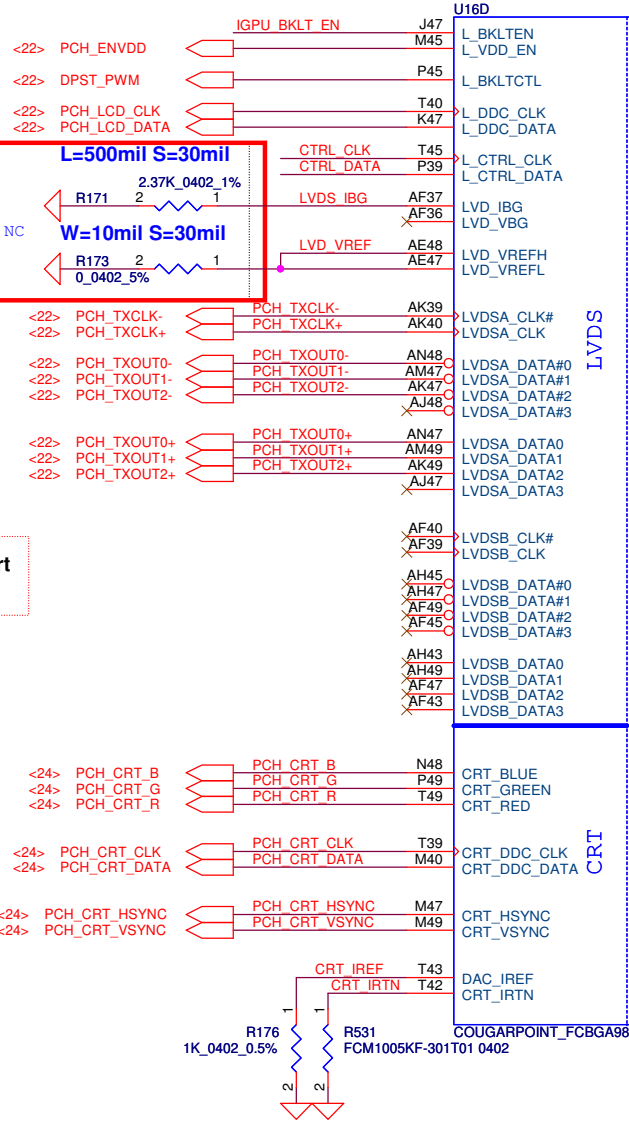
DIS only can NC

L=500mil S=30mil

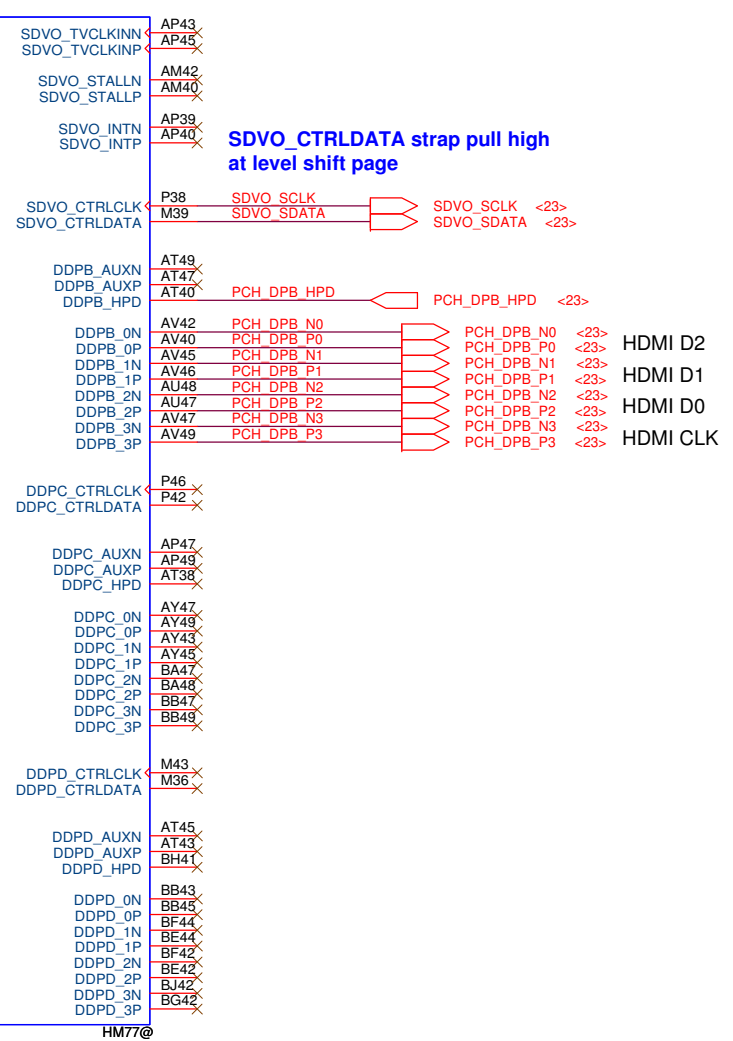
R171 2 2.37K_0402_1%

W=10mil S=30mil

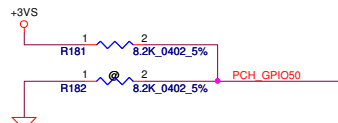
R173 2 0_0402_5%



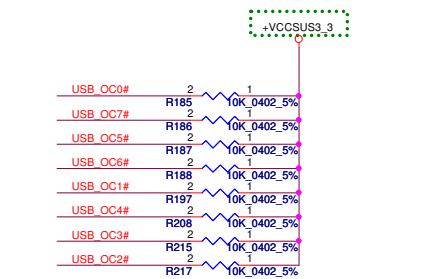
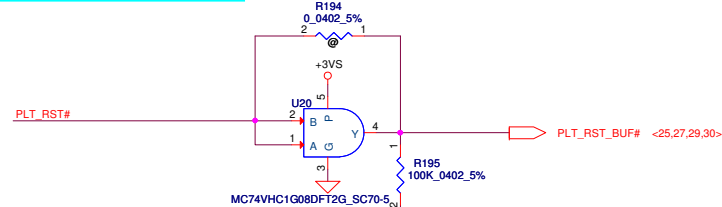
Digital Display Interface



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Issued Date	2012/03/21	Deciphered Date	2013/03/21	Title		
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				CHROME M/B LA-8943P Schematic		
				Date: Friday, August 10, 2012	Sheet 16 of 45	



CR Check list 1.5 only use for GPIO
無須PH(Internal PH),如做GPIO PU +3VS

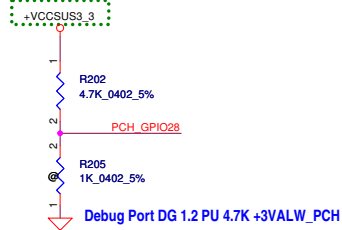


HDA_SYNC PH(PLL =+1.5VS)

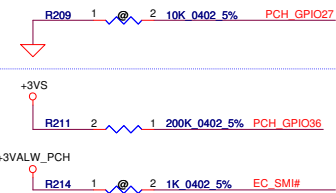
GPIO28

On-Die PLL Voltage Regulator

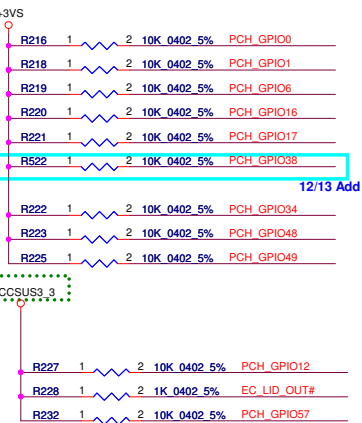
This signal has a weak internal pull up
 * H : On-Die PLL voltage regulator enable
 L : On-Die PLL Voltage Regulator disable



Deep S4,S5 wake event signal
 RTC alarm,Power BTN,GPIO27
 PCH_GPIO27 (Have internal Pull-High)
 Deep S4,S5 wake event signal



SATA2GP/GPIO36 & SATA3GP/GPIO37
 Sampled at Rising edge of PWROK.
 Weak internal pull-down.
 (weak internal pull-down is disabled
 after PLTRST# de-asserts)
 NOTE: This signal should NOT be
 pulled high when strap is sampled



12/13 Add

GPIO24 Unmultiplexed
 NOTE: GPIO24 configuration
 register bits are not cleared by
 CF9h reset event.
 CRB1.0 PU 10K to +3VALW

Fan Tachometer Inputs
 TACH1~7 only on server
 can insted to GPIO

No use PU 10K +3VS	PCH_GPIO00	T7
No use PU 10K +3VS	PCH_GPIO01	A42
No use PU 10K +3VS	PCH_GPIO06	H36
No use PU 10K +3VS	<29> EC_SCI#	EC_SCI#
No use PU 10K +3VALW	<29> EC_SMI#	EC_SMI#
No use PU +3VALW	<30> PCH_GPIO12	PCH_GPIO12
No use PU +3VALW	<29> EC_LID_OUT#	EC_LID_OUT#
No use PU +3VS	PCH_GPIO16	U2
No use PU +3VS <28,29> DEV_MODE	CRM@ 0 0402 5%	PCH_GPIO17
No use PU 10K +3VS	RAM flag	PCH_GPIO22
No use PU +3VALW	DDR3/DDR3L	PCH_GPIO24
No use PD 10K to GND	PCH_GPIO27	E16
No use PU 10K +3VALW	PCH_GPIO28	P8
No use PU 10K +3VS	BT ON/OFF	PCH_GPIO34
No use can NC	PAD T20 @	PCH_GPIO35
Can't PU	PAD T21 @	PCH_GPIO36
Can't PU	PAD T21 @	PCH_GPIO37
No use PU 10K +3VS	PCH_GPIO38	N2
No use PU 10K +3VS	RAM flag	PCH_GPIO39
No use PU 10K +3VS	PCH_GPIO48	V13
SATA5GP&TEMP_ALERT# CRB PU 10K +3VS	PCH_GPIO49	V3
No use PU +3VALW	PCH_GPIO57	D6

9/15 Layout
 request remove
 Test point
 They will route
 by itself

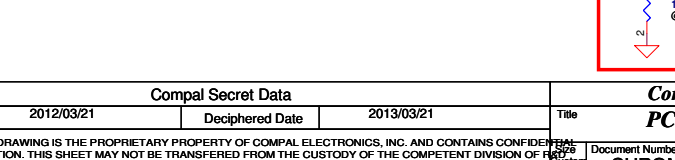
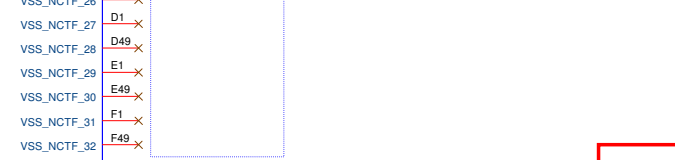
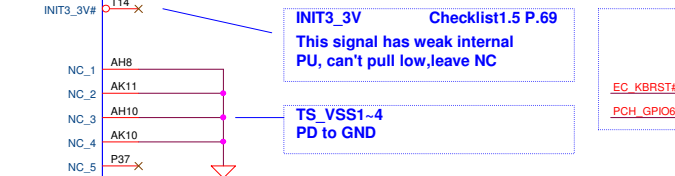
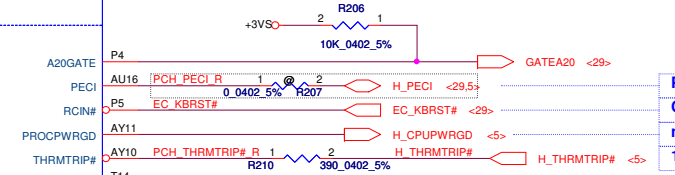
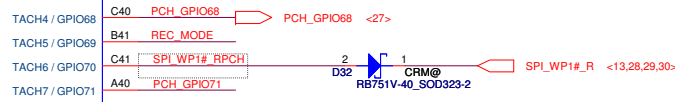
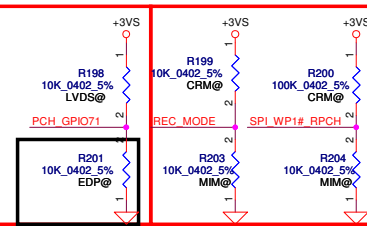
U16F	T7	BMBUSY# / GPIO0
A42	TACH1 / GPIO1	
H36	TACH2 / GPIO6	
E38	TACH3 / GPIO7	
C10	GPIO8	
C4	LAN_PHY_PWR_CTRL / GPIO12	
G2	GPIO15	
U2	SATA4GP / GPIO16	
D40	TACH0 / GPIO17	
T5	SCLOCK / GPIO22	
E8	GPIO24 / MEM_LED	
GPIO27	GPIO27	
P8	GPIO28	
K1	STP_PC# / GPIO34	
K4	GPIO35	
V8	SATA2GP / GPIO36	
M5	SATA3GP / GPIO37	
N2	SLOAD / GPIO38	
M3	SDATAOUT0 / GPIO39	
V13	SDATAOUT1 / GPIO48	
V3	SATA5GP / GPIO49	
D6	GPIO57	

A4	VSS_NCTF_1
A44	VSS_NCTF_2
A45	VSS_NCTF_3
A46	VSS_NCTF_4
A5	VSS_NCTF_5
A6	VSS_NCTF_6
B3	VSS_NCTF_7
B47	VSS_NCTF_8
BD1	VSS_NCTF_9
BD49	VSS_NCTF_10
BE1	VSS_NCTF_11
BE49	VSS_NCTF_12
BF1	VSS_NCTF_13
BF49	VSS_NCTF_14

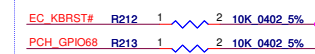
COUGARPOINT_FCBGA988
 HM77@

11/21 EDP@->POP

LVDS/eDP	GPIO71
LVDS	1
eDP	0



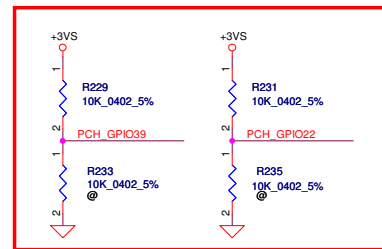
PECI CPU-EC
 CTRL+ALT+DEL
 non CPU power ok
 130c shut down



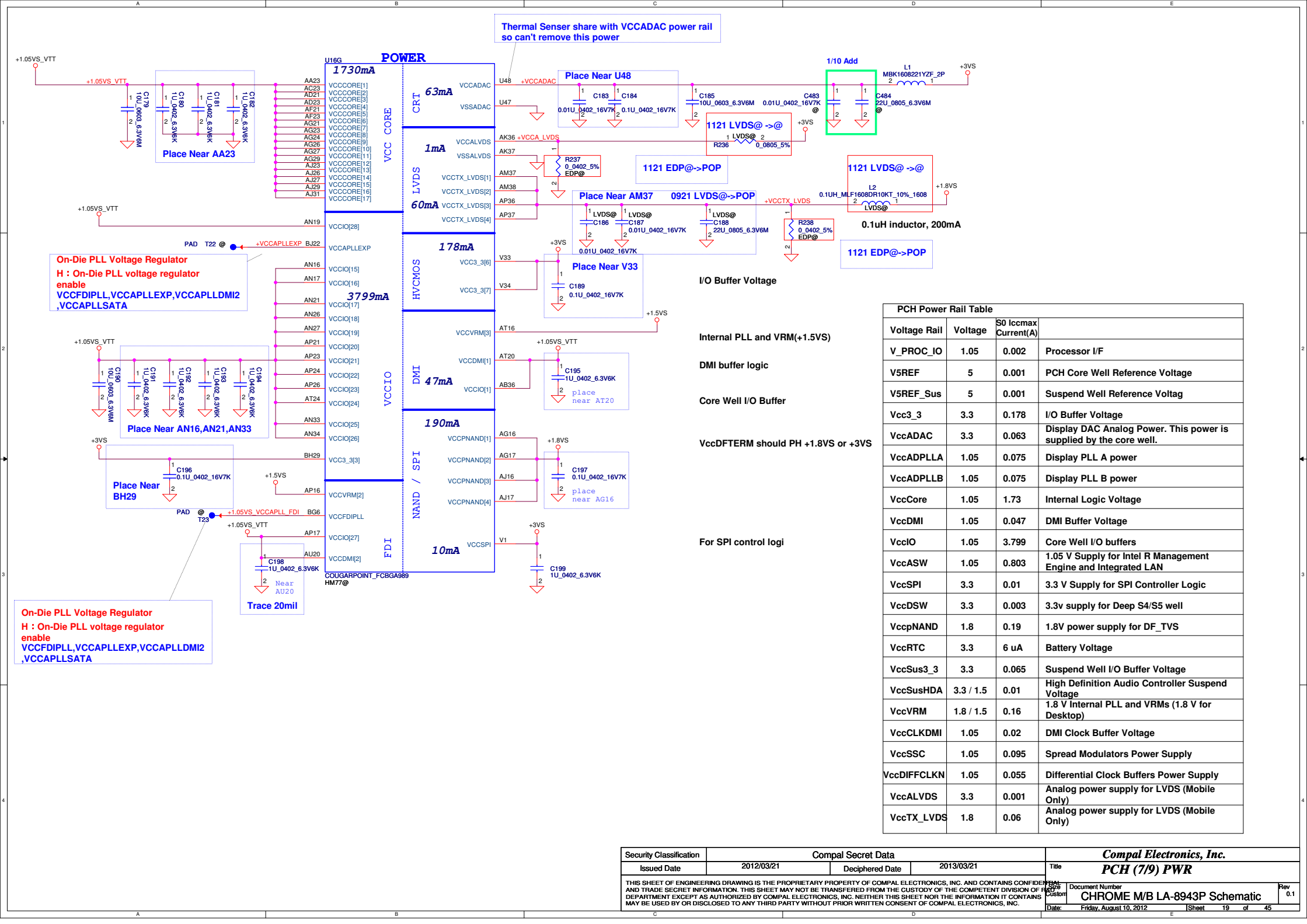
INIT3_3V
 Checklist1.5 P.69
 This signal has weak internal
 PU, can't pull low,leave NC

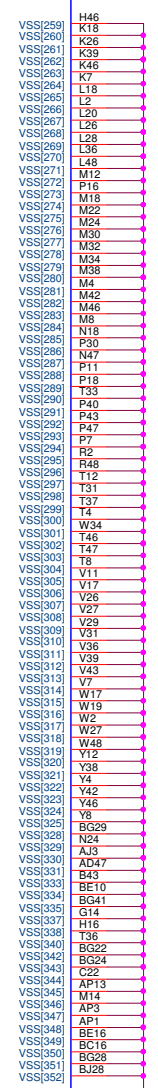
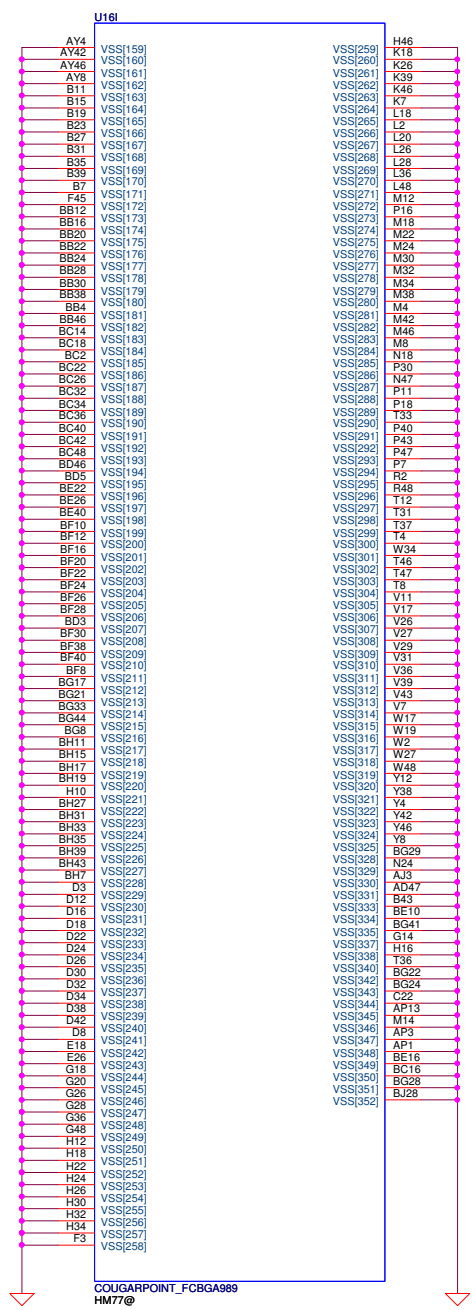
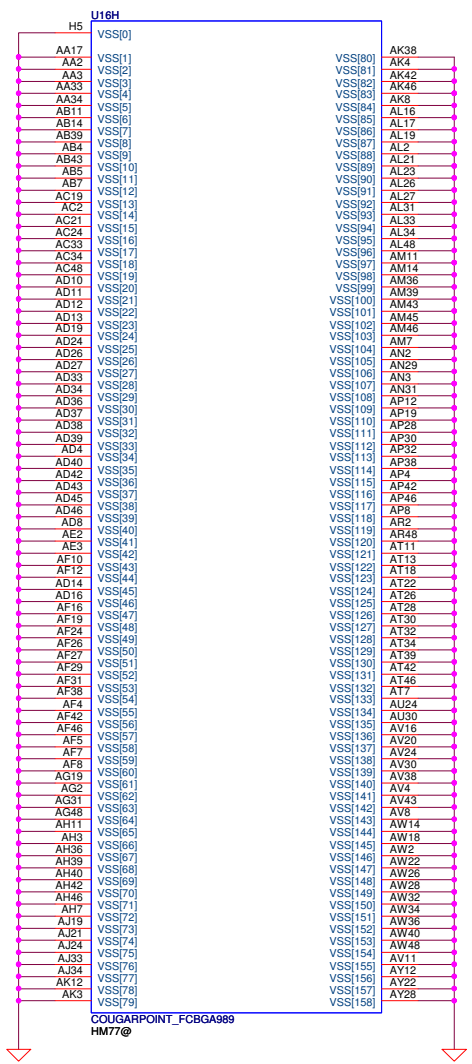
TS_VSS1~4
 PD to GND

9/15 Layout
 request remove
 Test point
 They will route
 by itself



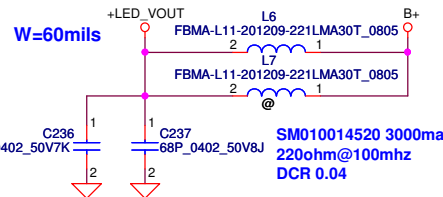
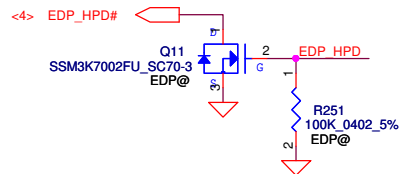
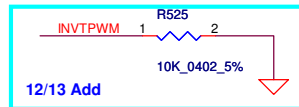
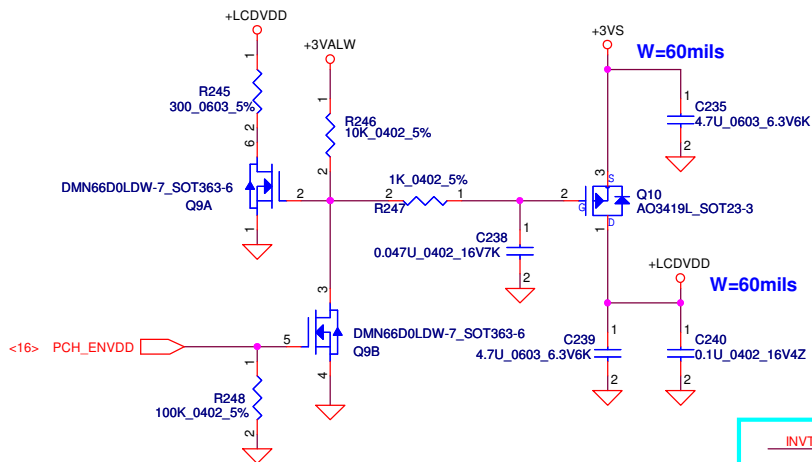
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					CHROME M/B LA-8943P Schematic
					Rev 0.1
					Date: Friday, August 10, 2012
					Sheet 18 of 45



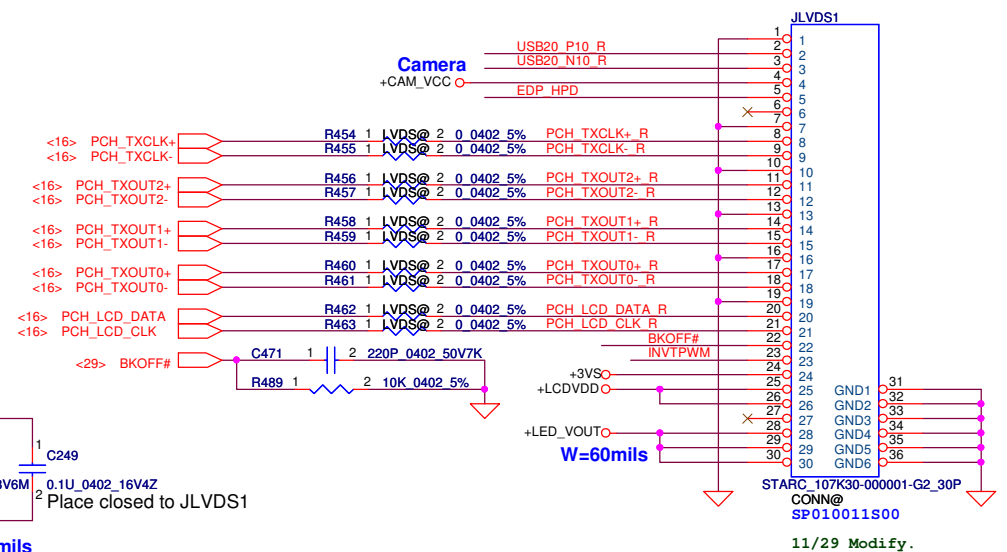


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				CHROME M/B LA-8943P Schematic	0.1
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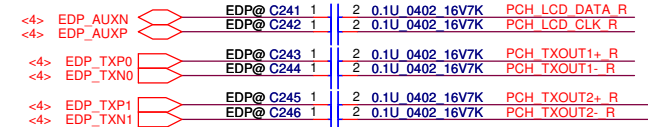
LCD POWER CIRCUIT



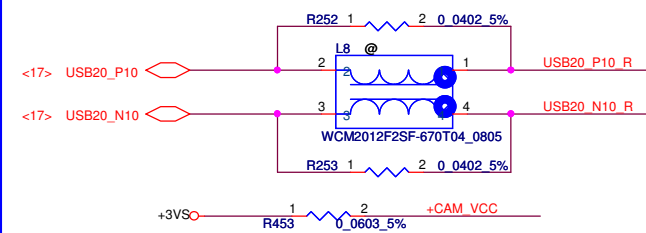
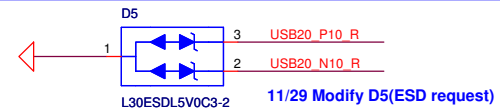
LCD/LED PANEL Conn.



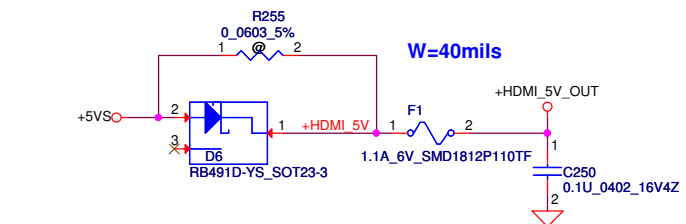
eDP



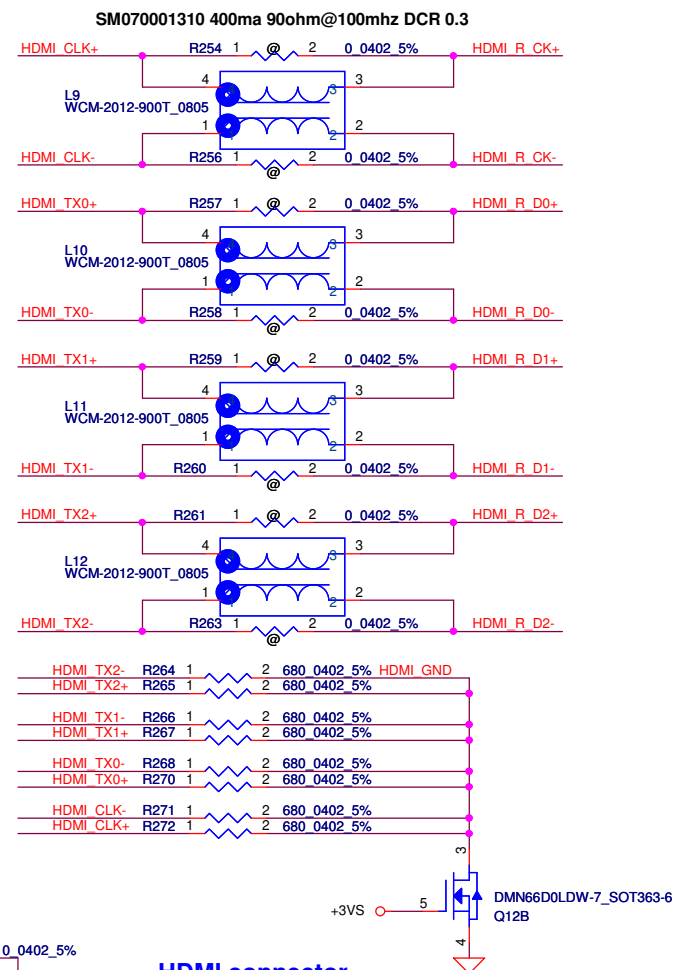
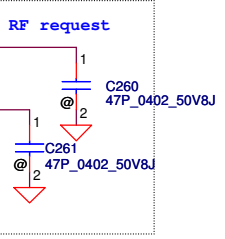
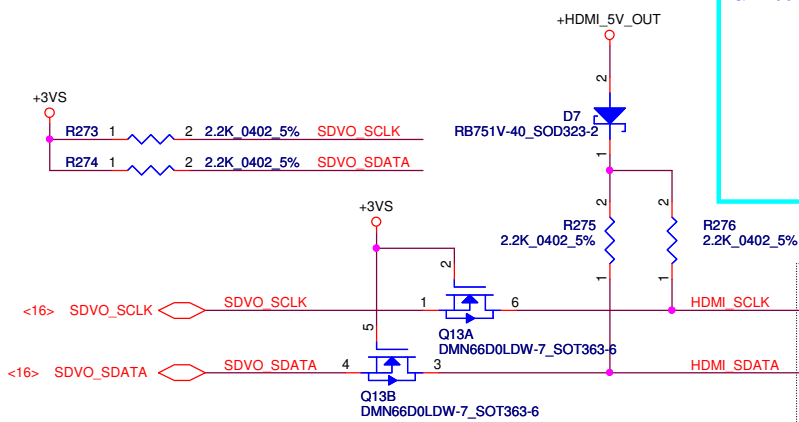
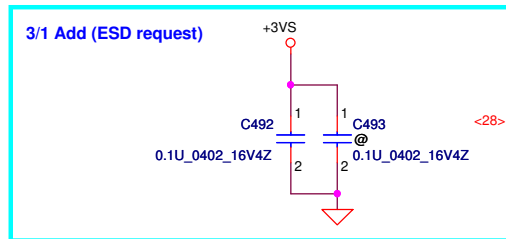
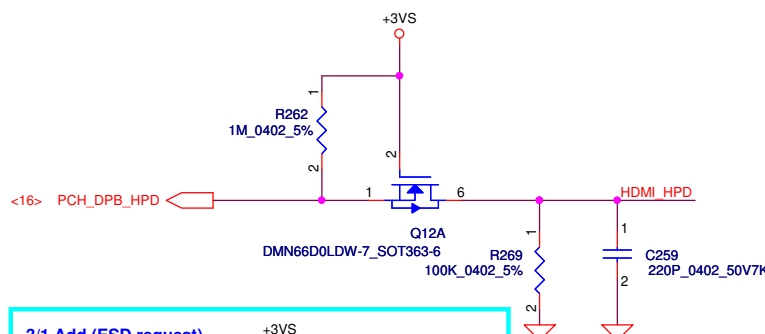
Camera



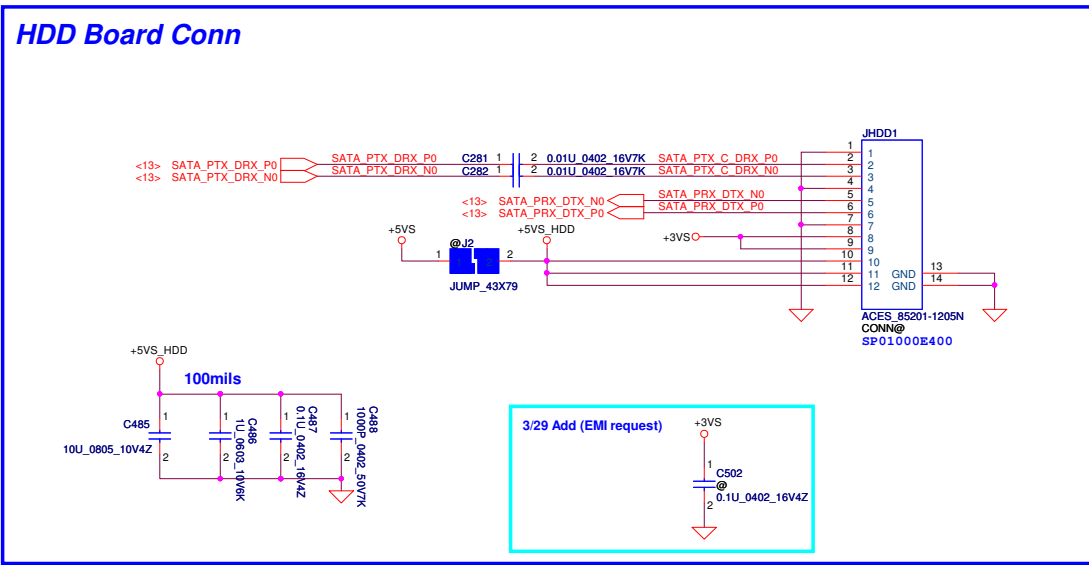
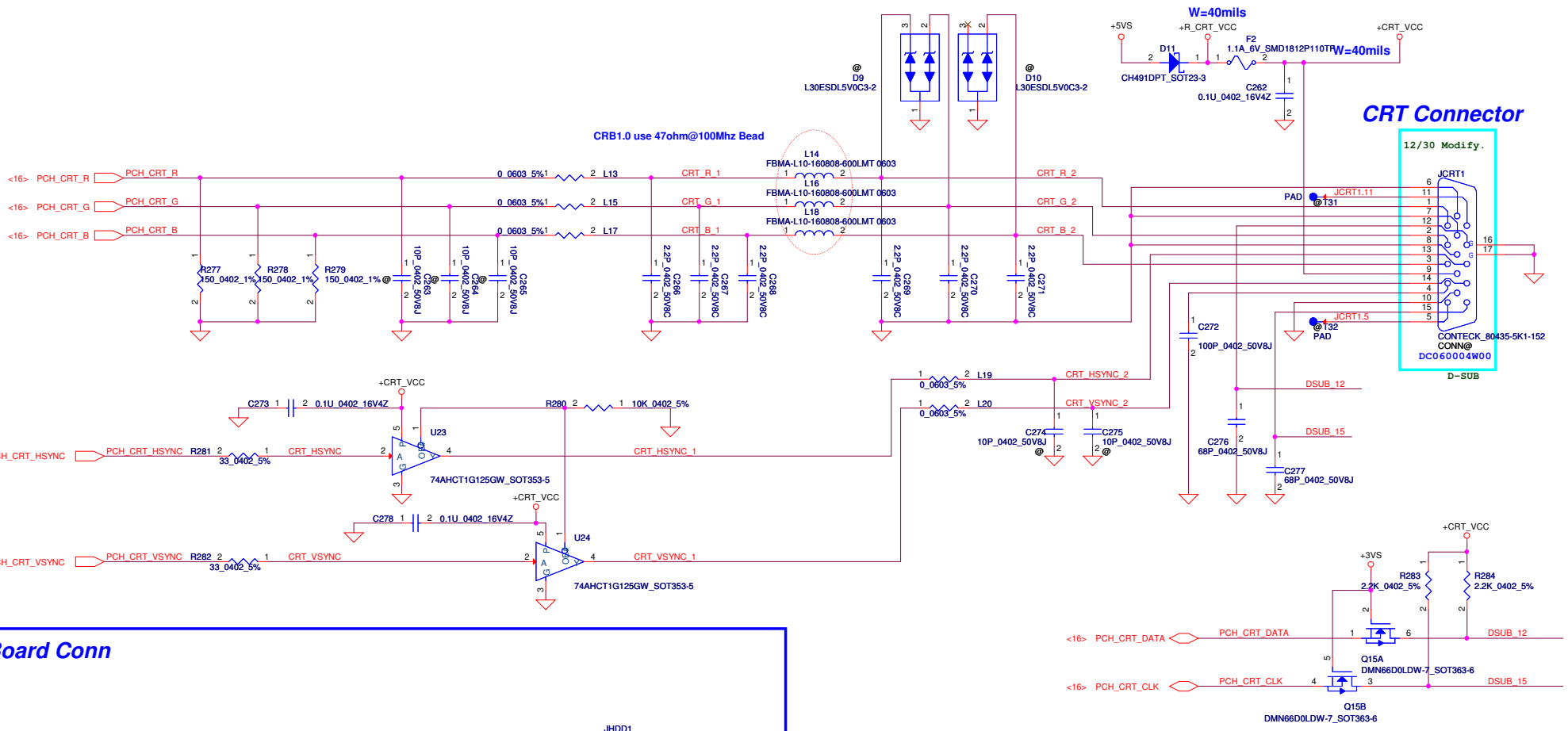
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				Date	Friday, August 10, 2012
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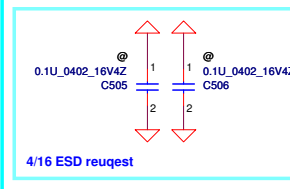
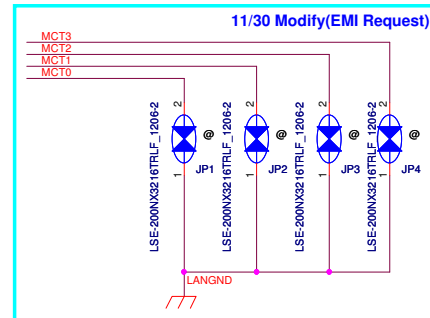
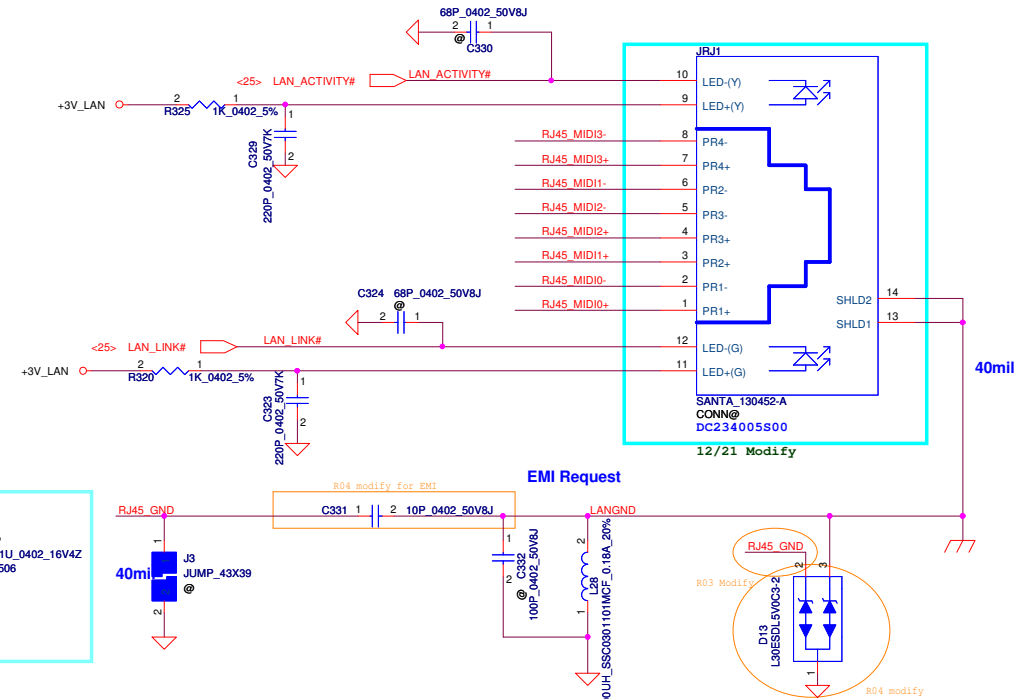
<16> PCH_DPB_N0	C251	2	1	0.1U_0402_16V7K	HDMI TX2-
<16> PCH_DPB_P0	C252	2	1	0.1U_0402_16V7K	HDMI TX2+
<16> PCH_DPB_N1	C253	2	1	0.1U_0402_16V7K	HDMI TX1-
<16> PCH_DPB_P1	C254	2	1	0.1U_0402_16V7K	HDMI TX1+
<16> PCH_DPB_N2	C255	2	1	0.1U_0402_16V7K	HDMI TX0-
<16> PCH_DPB_P2	C256	2	1	0.1U_0402_16V7K	HDMI TX0+
<16> PCH_DPB_N3	C257	2	1	0.1U_0402_16V7K	HDMI CLK-
<16> PCH_DPB_P3	C258	2	1	0.1U_0402_16V7K	HDMI CLK+



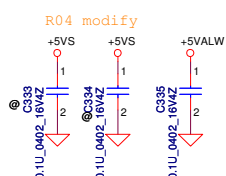
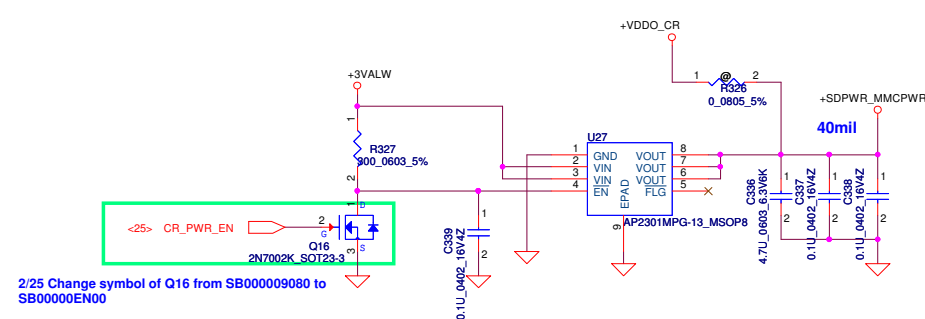
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				Size Document Number
				Custom CHROME M/B LA-8943P Schematic
				Rev 0.1
				Date: Friday, August 10, 2012
				Sheet 23 of 45



C474,C475 and D14
ME interfere,do not pop!!

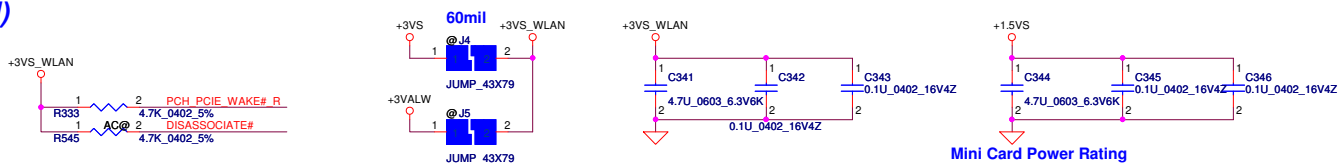


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				Document Number	0.1
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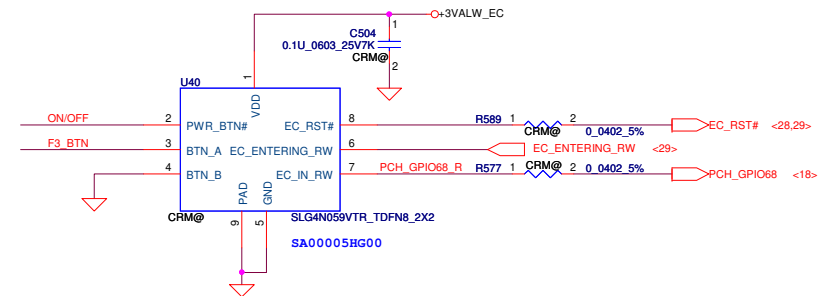
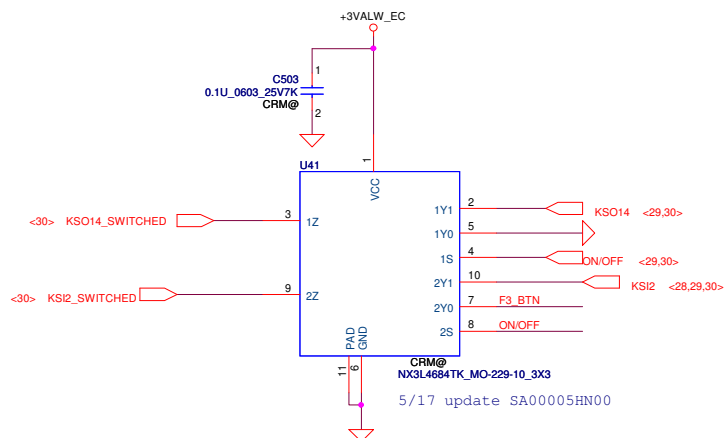
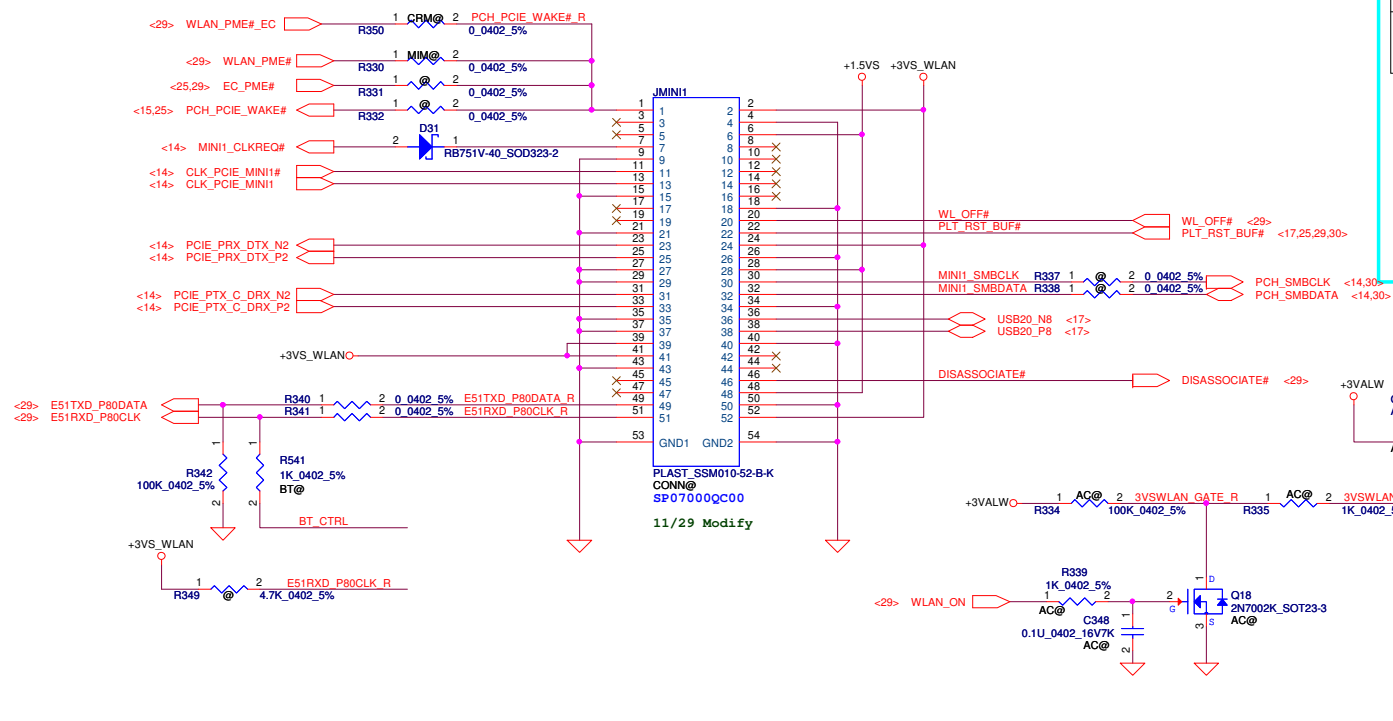
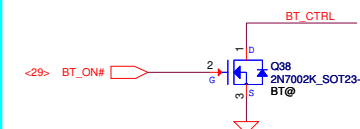
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Mini Card Power Rating

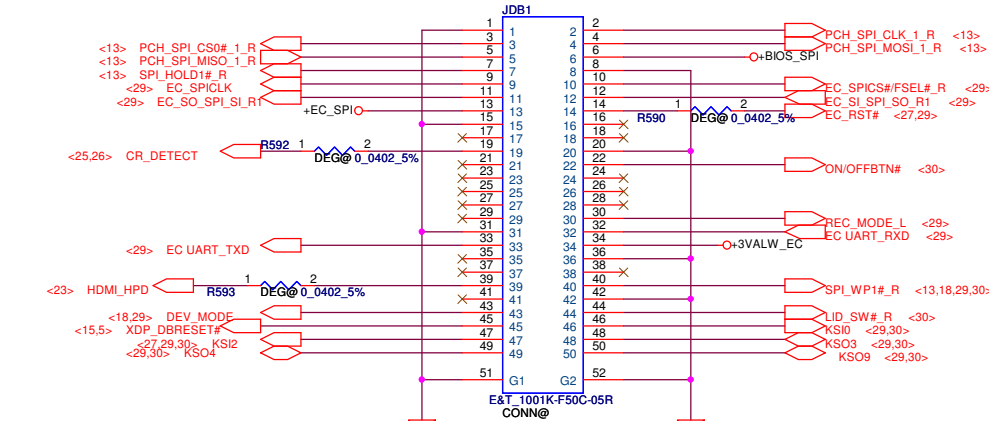
WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CTRL	H	L
BT_ON#	L	H

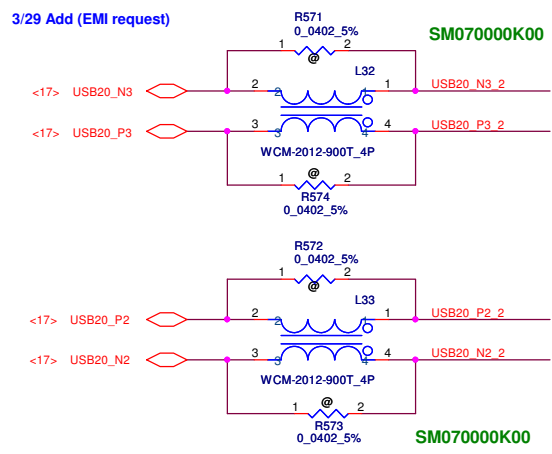


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				Size	Document Number	Rev
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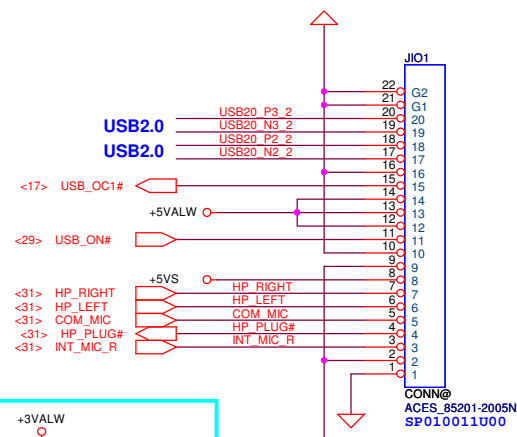
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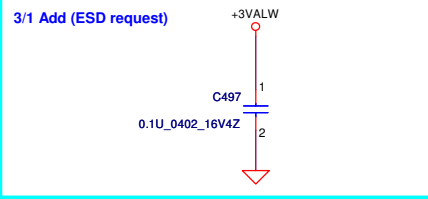
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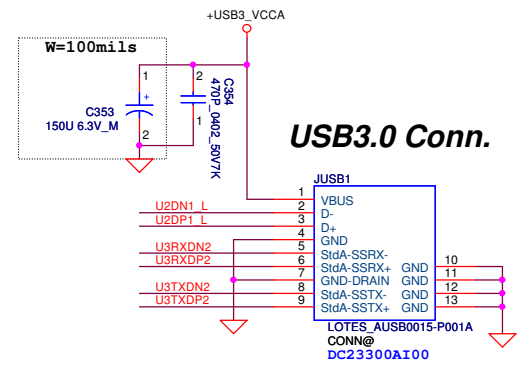
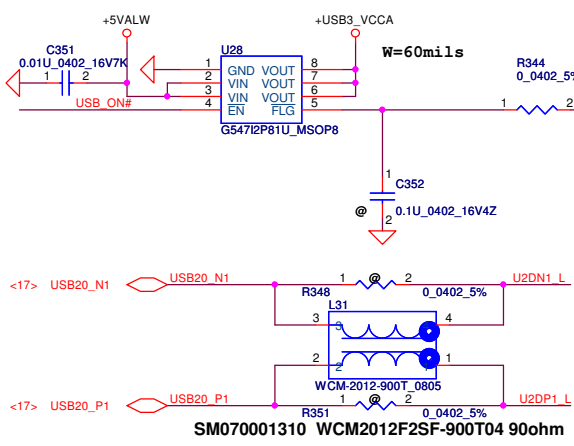
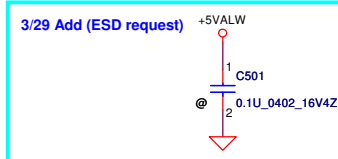
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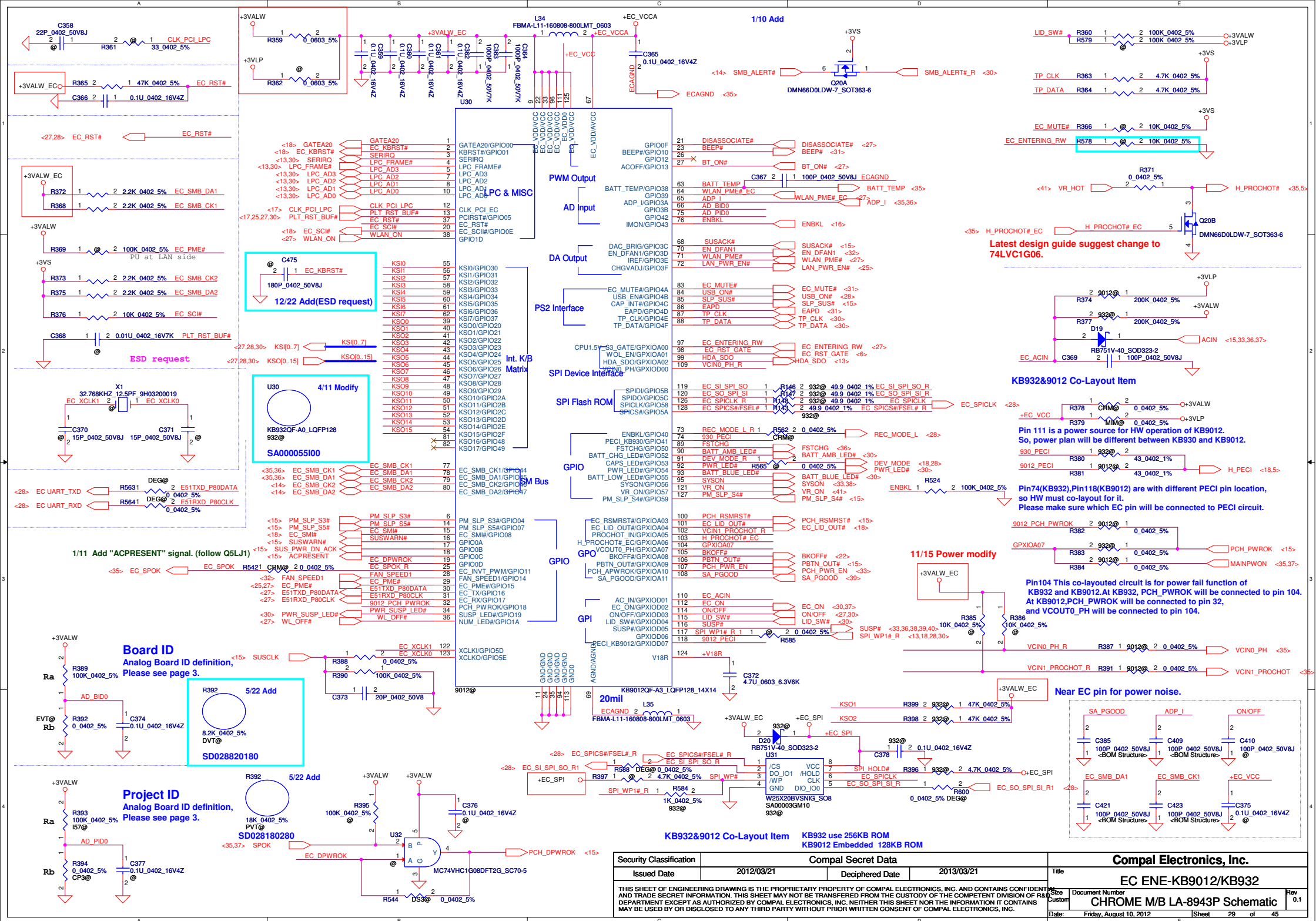
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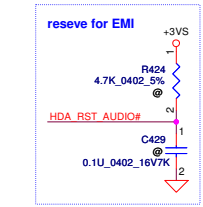
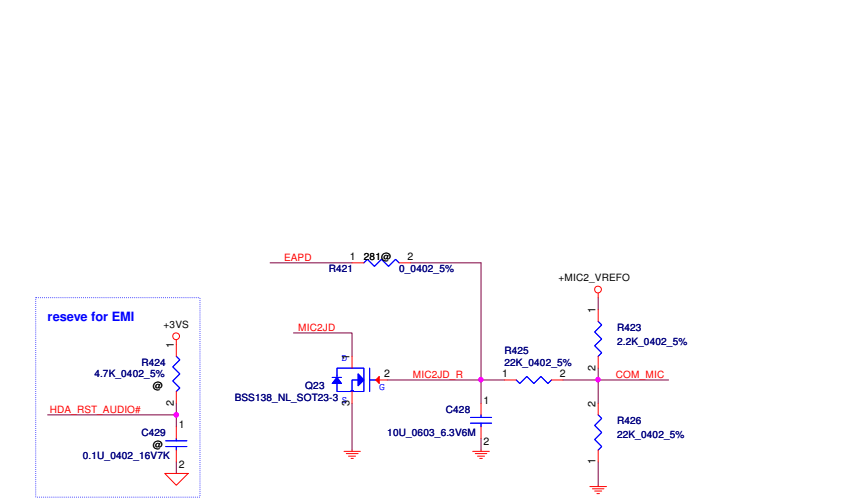
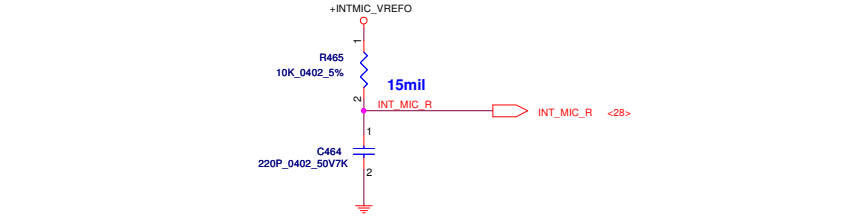
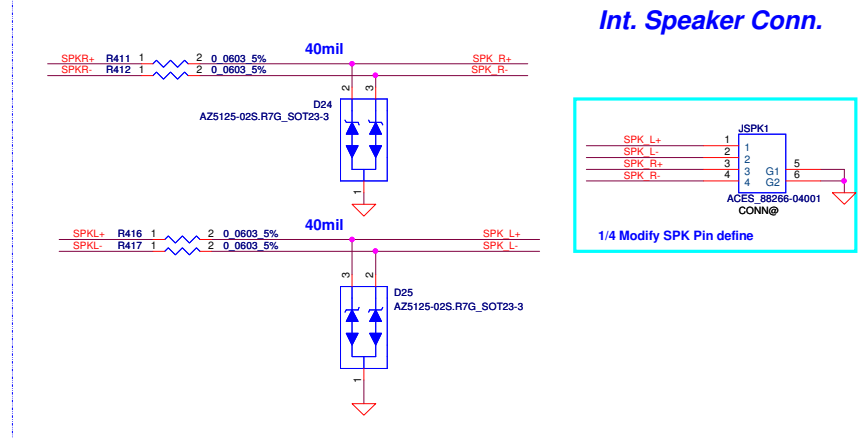
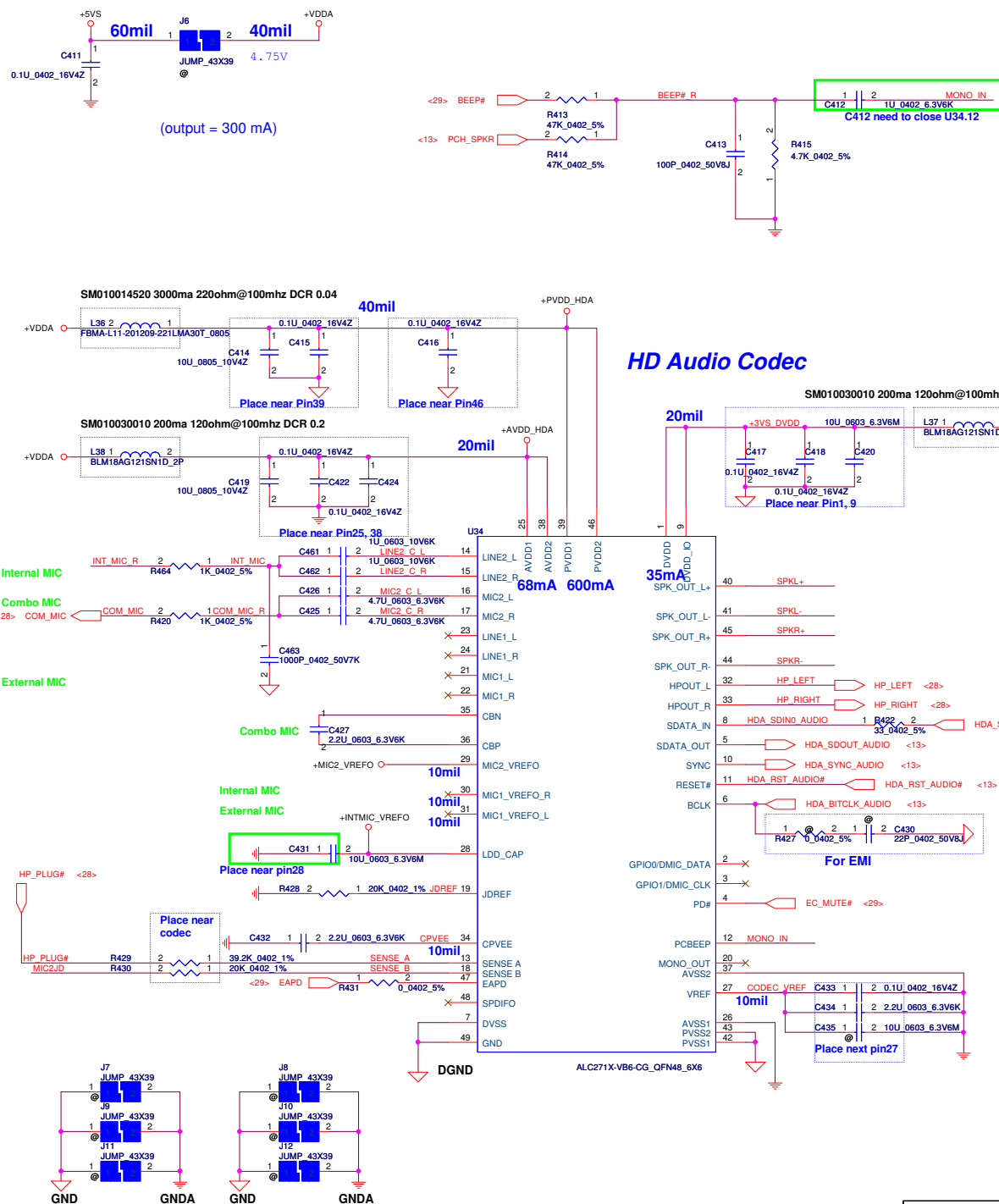
USB3.0



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Issued Date	2012/03/21	Deciphered Date	2013/03/21	IO Board & USB3.0	
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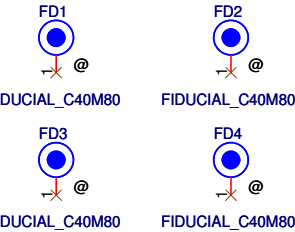
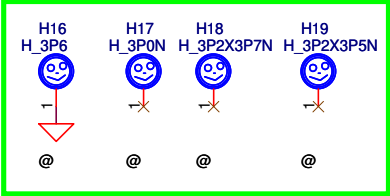
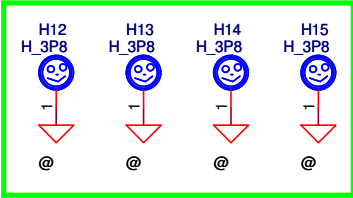
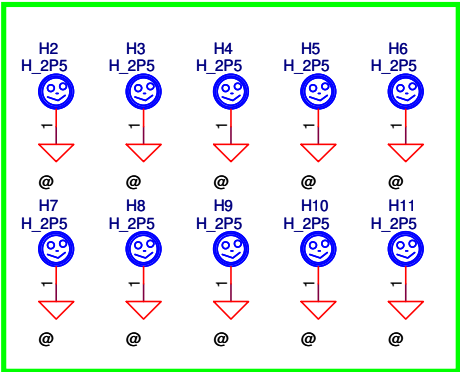
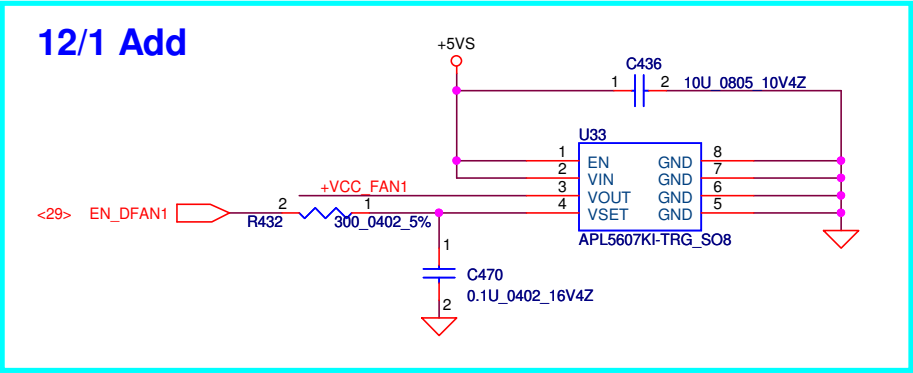
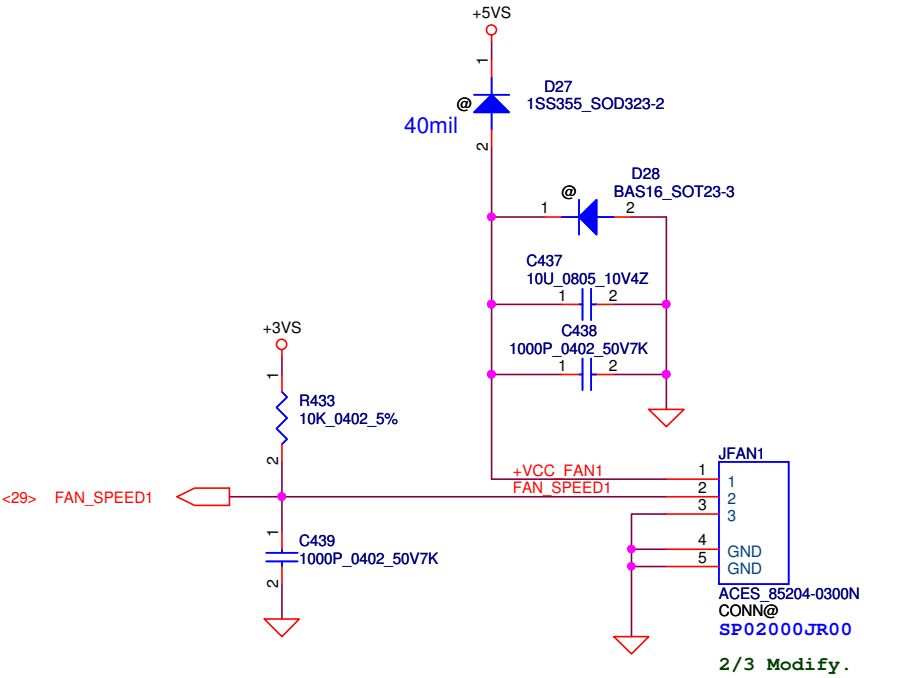


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				Custom	CHROME M/B LA-8943P Schematic	0.1
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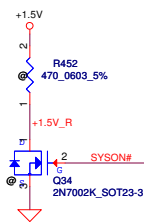
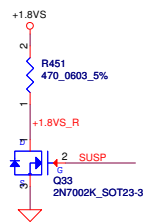
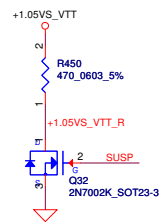
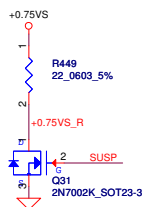
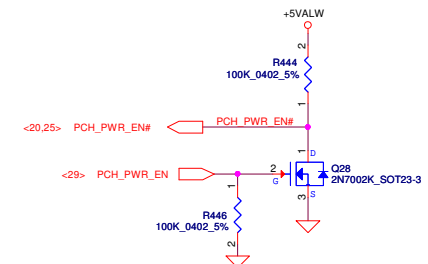
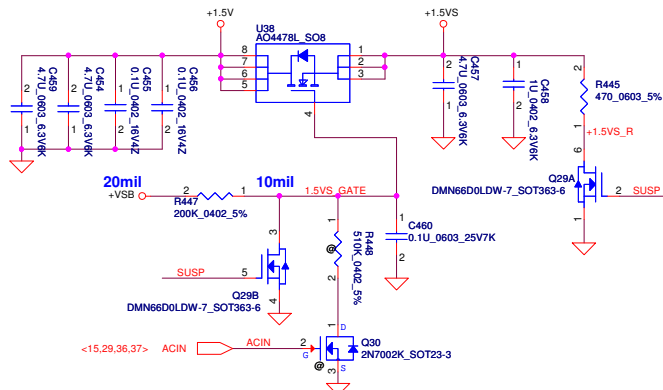
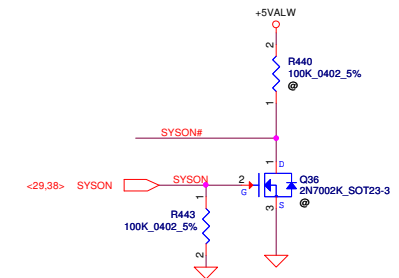
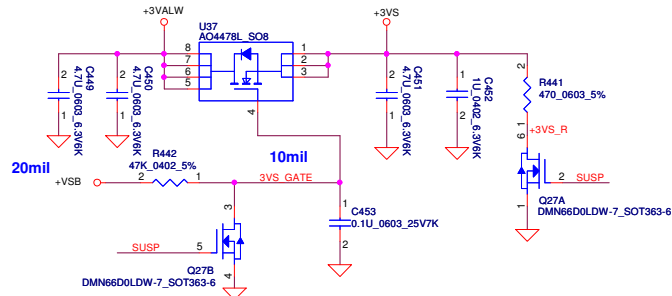
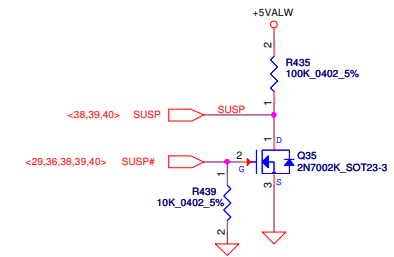
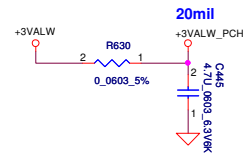
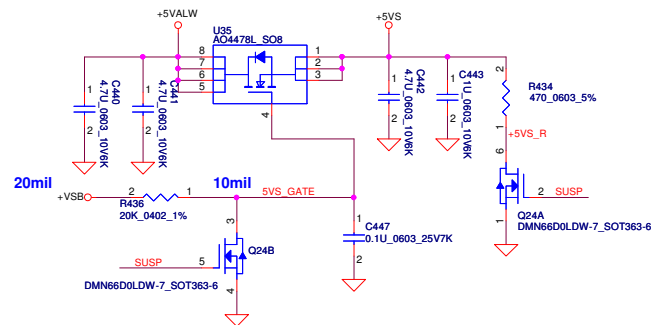
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Size	Custom	Document Number	CHROME M/B LA-8943P Schematic	Rev	0.1
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FAN1 Conn

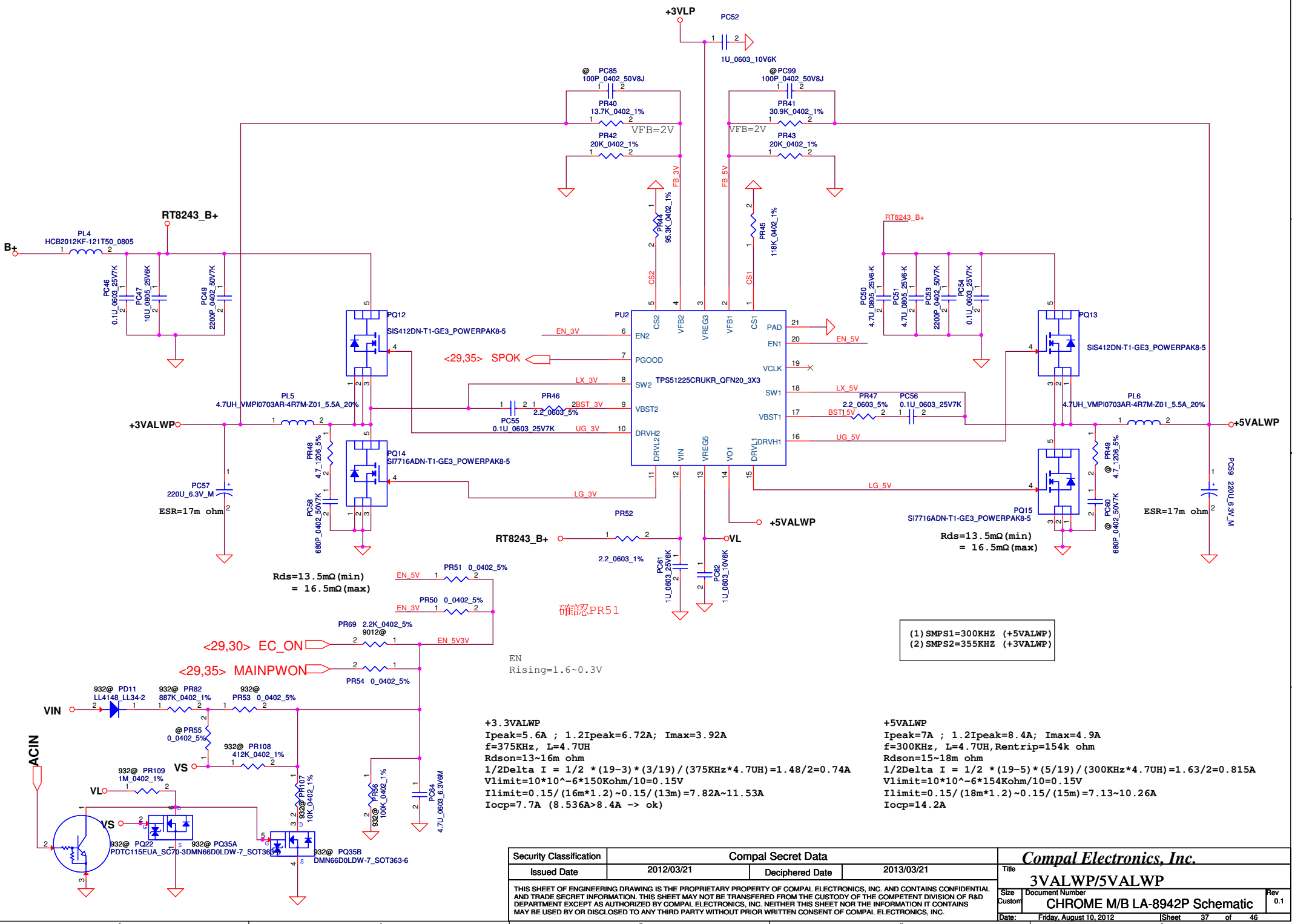


CPU support plate

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						Size	Document Number			Rev		
						Custom	CHROME M/B LA-8943P Schematic			0.1		
						Date:	Friday, August 10, 2012		Sheet	32	of	45



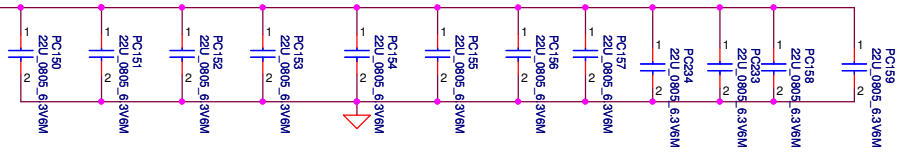
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Issued Date	2012/03/21	Deciphered Date	2013/03/21	DC Interface				
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				Size	Document Number	CHROME M/B LA-8943P Schematic		Rev 0.1
				Customer				
				Date:	Friday, August 10, 2012	Sheet	33 of 45	



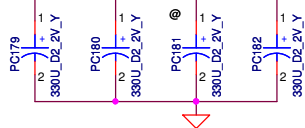
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					3VALWP/5VALWP	
Size		Document Number		Rev		
Custom		CHROME M/B LA-8942P Schematic		0.1		
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CR PDDG Rev 0.95

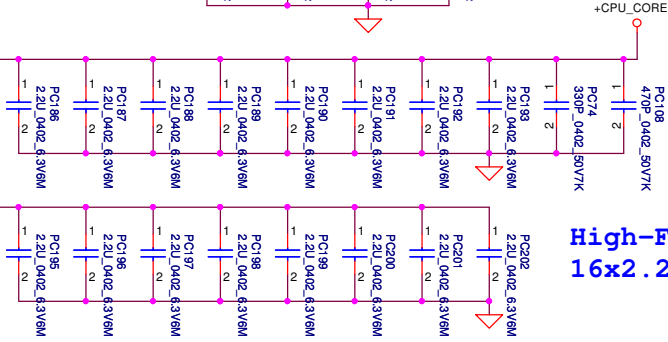
Mid-Frequency Decoupling 12x22 μ F



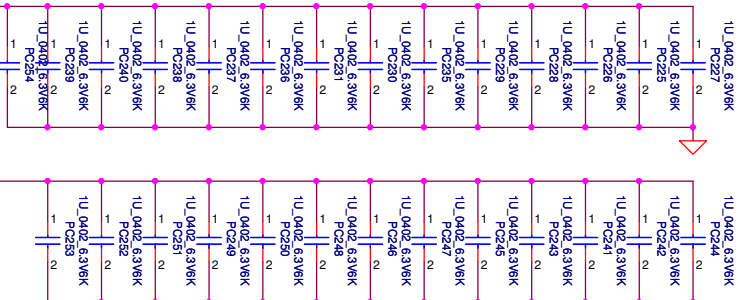
Low-Frequency Decoupling 3x330 μ F 9m



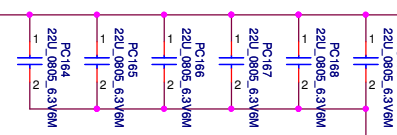
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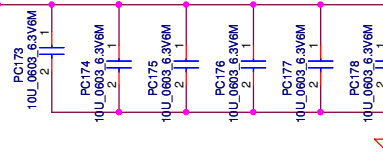
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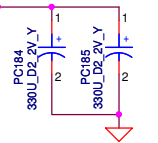
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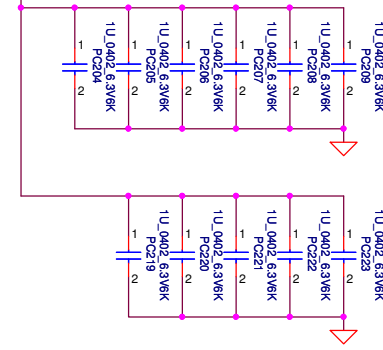
Mid-Frequency Decoupling 6x10 μ F 0603



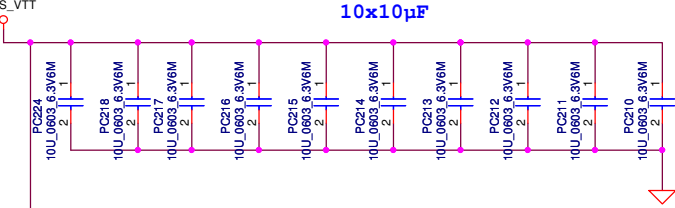
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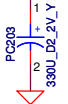
High-Frequency Decoupling 11x1 μ F



Mid-Frequency Decoupling 10x10 μ F



Low-Frequency Decoupling 1x330 μ F 9m



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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Modify DCIN/Pre-change power circuit	0.1	34	Add PC301 330P_0402_50V7K, PC302 470P_0402_50V7K for EMI solution	2012/4/5	EVT
2		Modify Battery CONN/OTP power circuit	0.1	35	Add PR80 0ohm to GND for BOM control (9012 AGND)	2012/4/5	EVT
3		Modify CHARGER	0.1	36	Add PC16,PC63 330P_0402_50V7K, PC20, PC48 470P_0402_50V7K, PC113, PC114, PC115, PC117, PC121 0.1U_0402_25V6 PR26 4.7_1206_5%, PC39 680P_0402_50V7K for EMI solution	2012/4/5	EVT
4		Modify 3VALWP/5VALWP power circuit	0.1	37	Add Snubber PR48 4.7_1206_5%, PC58 680P_0402_50V7K for EMI solution	2012/4/5	EVT
5		Modify 1.5VP/0.75VSP power circuit	0.1	38	Add Snubber PR175 4.7_1206_5%, PC75 680P_0402_50V7K for EMI solution	2012/4/5	EVT
6		Modify 1.05VS power circuit	0.1	40	Delete PR105 5.1K_0402_1%; PR178 0_0402_5%, Add PR188 4.99K_0402_1%; PR186 1.2K_0402_1%, PC122 1000P_0402_50V7K; PC124 0.1U_0402_25V6 for improve load response	2012/4/5	EVT
7		Modify CPU/GFX_CORE power circuit	0.1	41	Add PC45 330P_0402_50V7K, PC21 470P_0402_50V7K for EMI solution Add PC169 0.047I_0402_25V7K, change PR187 from 523 to 348_0402_1% change PR135 from 412 to 430_0402_1%	2012/4/5	EVT
8		Modify CPU/GFX_CORE power circuit	0.1	41	change PL14 from 0.22U_PCMB104T-R22MS_35A_20% to 0.22UH MMD-10RCZ-R22M-28A (from H=3 to H=4) change PR201, PR152 from 27.4K to 61.9K_0402_1%, change PH4,PH5 470K_0402_5%(from Thinking to Panasonic) thermal issue	2012/4/5	EVT
9		Modify PROCESSOR DECOUPLING power circuit	0.1	42	Add PC74 330P_0402_50V7K, PC108 470P_0402_50V7K for EMI solution	2012/4/5	EVT
10		Modify DCIN/Pre-change power circuit	0.1	34	Sawp PC10 and PC301; Sawp PC14 and PC302	2012/4/5	EVT
11		Modify Battery CONN/OTP power circuit	0.1	35	Add PR105 0ohm to GND for BOM control (9012 H_PROCHOT#_EC) change PR61 from 21K to 21.5K and PR66 from 9.53K to 9.76K for 92 throttling and 56C recovery	2012/4/18	EVT
12		Modify Battery CONN/OTP power circuit	0.1	35	Delete PR78 and add PR61, PR63 for EC932, change PR66 from 9.53kohm to 9.76k ohm, OTP setting 92C thermal protection, 56C recovery	2012/4/26	EVT
13		Modify 3VALWP/5VALWP power circuit	0.1	37	Change PR56 from 402K to 100K for 3V/5V enable setting, Add PR53 for 3V/5V enable setting.	2012/4/26	EVT
14		Modify CPU/GFX_CORE power circuit	0.1	41	change PR187 from 348 to 324 for OCP 40A fine tune, change PC169 from 0.047U to 0.068U (RC match)	2012/4/26	EVT
15		Modify CHARGER	0.1	36	change PC22 from 0.1U_0402_25V6 to 330P_0402_50V7K	2012/5/2	EVT

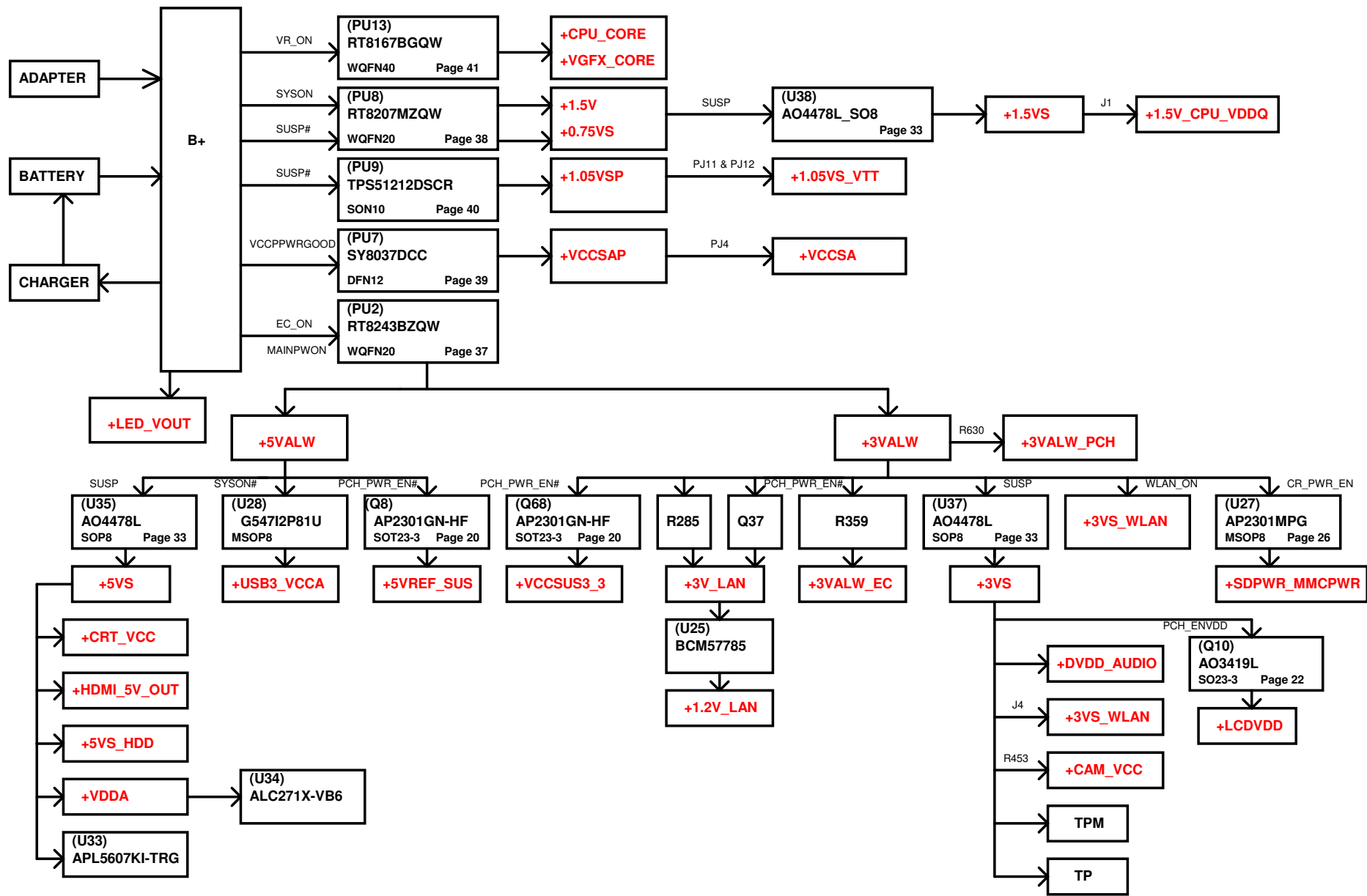
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Issued Date	2012/03/21	Deciphered Date	2013/03/21	Title	PIR1 (PWR)
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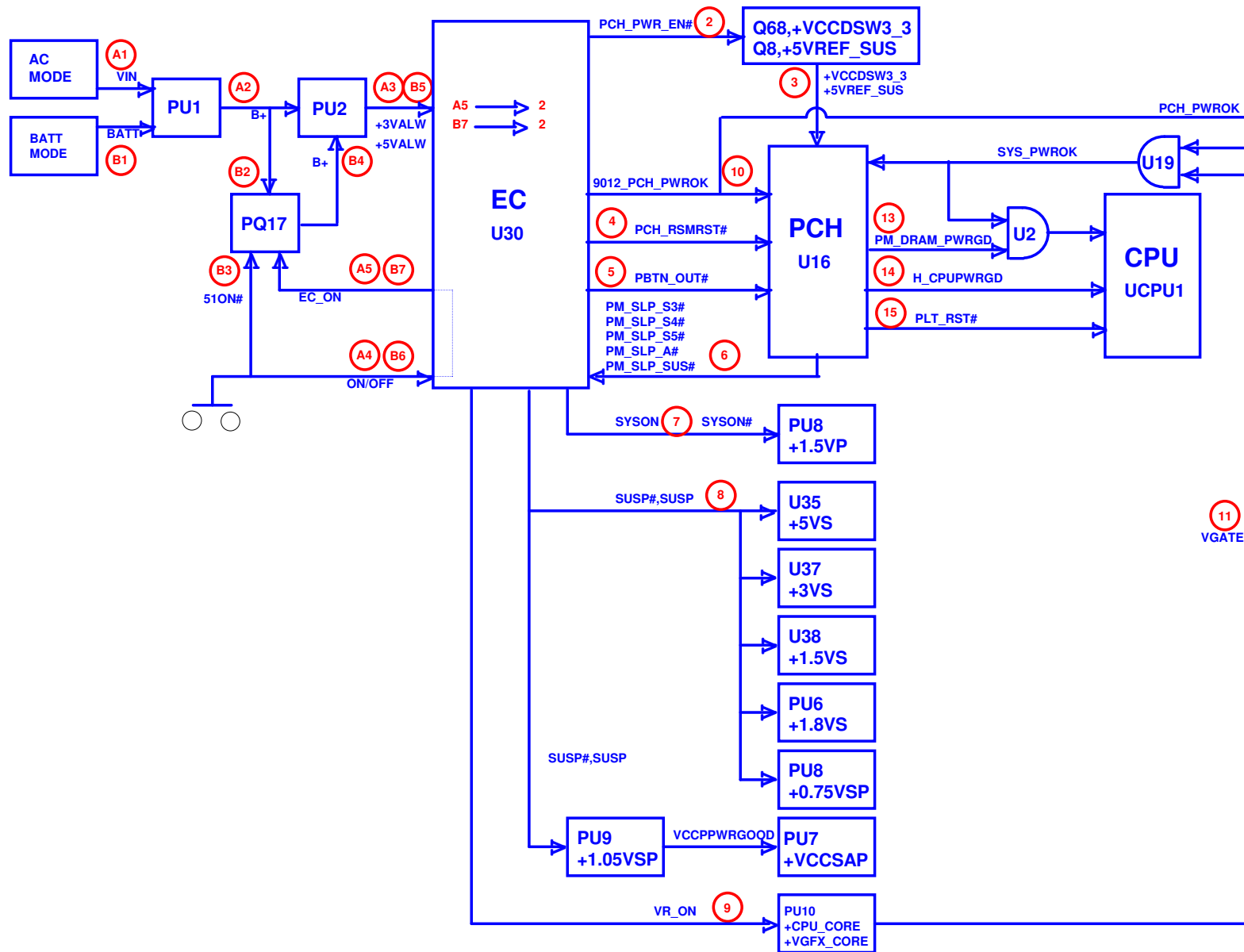
Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Modify Prochot# setting from KB9012 to G718(EVT MEMO introction)	0.2	35	change PR63 from 2.26K to 590 ohm, PR68 from 9.1 to 1.91K From 46.2W~38W to 42.8W~33.2W	2012/5/7	EVT
2		Modify Battery CONN/OTP power circuit Modify 3VALWP/5VALWP power circuit	0.2	35 37	Sawp PR81 and PR82 location leverage Mimic winsows	2012/5/17	DVT
3		Modify Battery CONN/OTP power circuit	0.2	35	Add PR111 between 3VLP and battery connect TH for EC932	2012/5/23	DVT
4		Remove PQ16 PC302 PR10 PR11	0.2	34	Remove 51ON# RC, BATT+ to VS switch	2012/5/23	
5		MAINPWON double pull high.	0.2	35	Remove PR64	2012/5/23	
6		Modify 3v5v EN pin voltage (from 4.9V to 4.524V) for EN pin rating.	0.2	35	Change PR108 from 316K to 412K.	2012/5/23	
7		Modify 3v5v EN pin voltage for EN pin rating.	0.3	35	Change PR82 from 1000K to 887K.	2012/7/9	PVT
8							
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